Date: April. 6, 2012

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A001C/E	Rev.	3.00
Title	Correction for Incorrect Description Notice RL78/G13 Descriptions in the Hardware User's Manual Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G13 Group R5F100xxx, R5F101xxx	Lot No. All lot	Reference Document	RL78/G13 User's Manual: Hardware Rev. 1.00 R01UH0146EJ0100 (Sep. 2011)		

This document describes misstatements found in the RL78 hardware user's manual Rev. 1.00 (R01UH0146EJ0100).

Corrections

User's Manual Applicable Page	Applicable Item	Contents
Pages 5, 988	Industrial applications and extended-temperature products released	Products released
Page 93	Incorrect descriptions of recommended connection of unused pins of P60 to P63 in table2-3 in pin functions chapter revised	Incorrect descriptions revised
Page 449	Incorrect descriptions of 7.4.2 Shifting to HALT/STOP mode after starting operation, in real-time clock chapter revised	Incorrect descriptions revised
Pages 308, 860, 861, 864 to 867, 871, 872, 883, 884	Incorrect descriptions of reset processing time/standby mode release time revised	Incorrect descriptions revised
Pages 493, 494, 526	Explanations of when using SNOOZE mode in A/D converter chapter added	Explanations added
Pages 631, 633, 658, 659, 661	Caution of when using SNOOZE mode in serial array unit chapter added	Caution added
Page 938	Explanations of data flash in flash memory chapter added	Explanations added
Page 983	Spec of on-chip oscillator characteristics in electrical specifications chapter confirmed	Spec confirmed

Incorrect: **Bold with underline**; Correct: Gray hatched

Document Improvement

The above corrections will be made for the next revision of the hardware user's manual around March, 2012. Contact a Renesas Electronics sales department details on the publishing schedule.

Corrections in the hardware user's manual

No.	Applicable Item			Rev 1.00	After Rev 2.00 Note
		Document No.	Japanese	R01UH0146JJ0100	R01UH0146JJ0200
			English	R01UH0146EJ0100	R01UH0146EJ0200
1	Incorrect descriptions of 64-pin plastic TQFP (7 x 7) deleted			–	✓
2	Incorrect descriptions of count registers, in real-time clock deleted			–	✓
3	Explanations of interval timer control register (ITMC) added			–	✓
4	Explanations of timing chart when A/D voltage comparator is used added			–	✓
5	Incorrect descriptions of A/D conversion time selection, there is stabilization wait time (6/8) to (8/8) revised			–	✓
6	Explanations when entering A/D converter standby mode added			–	✓
7	Incorrect descriptions of maskable interrupt request acknowledgment operation			–	✓
8	Incorrect descriptions of voltage detector (LVD) timing chart revised			–	✓
9	Incorrect descriptions of voltage detector (LVD) interrupt and reset mode revised			–	✓
10	Number (4) of Supply current characteristics in Electrical specifications chapter (section 29.4.2) is the same for all RL78/G13 Group products.			–	✓
11	Explanations when using temperature sensor and internal reference voltage (1.45 V) of A/D converter added			–	✓
12	Explanations when using temperature sensor and internal reference voltage (1.45 V) of A/D test function in Safety functions chapter added			–	✓
13	Conditions of A/D converter characteristics in Electrical specifications chapter (section 29.7.1) added			–	✓
14	Condition of Temperature sensor characteristics in Electrical specifications chapter (section 29.7.2) added			–	✓
15	**Industrial applications and extended-temperature products released**			–	✓
16	**Incorrect descriptions of recommended connection of unused pins of P60 to P63 in table2-3 in pin functions chapter revised**			–	✓
17	**Incorrect descriptions of 7.4.2 Shifting to HALT/STOP mode after starting operation, in real-time clock chapter revised**			–	✓
18	**Incorrect descriptions of reset processing time/standby mode release time revised**			–	✓
19	**Explanations of when using SNOOZE mode in A/D converter chapter added**			–	✓
20	**Caution of when using SNOOZE mode in serial array unit chapter added**			–	✓
21	**Explanations of data flash in flash memory chapter added**			–	✓
22	**Spec of on-chip oscillator characteristics in electrical specifications chapter confirmed**			–	✓

Note No.15 to 23 (bold text) are the corrections added in this notice.

Remarks ✓: Corrected

–: Items should be corrected

1. Descriptions of related information according to discontinued development of 64-pin plastic TQFP (7 x 7) package deleted

Order information of 64-pin plastic TQFP (7 x 7) deleted (page 4)

Incorrect: (2/3)

<table>
<tr><th>Pin count</th><th>Package</th><th>Data flash</th><th>Part Number</th></tr>
<tr><td colspan="4">(Omitted)</td></tr>
<tr><td rowspan="8">64 pins</td><td rowspan="2">64-pin plastic LQFP (12x12)</td><td>Mounted</td><td>R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA, R5F100LKAFA, R5F100LLAFA</td></tr>
<tr><td>Not mounted</td><td>R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA, R5F101LKAFA, R5F101LLAFA</td></tr>
<tr><td rowspan="2">64-pin plastic LQFP (fine pitch) (10 × 10)</td><td>Mounted</td><td>R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB</td></tr>
<tr><td>Not mounted</td><td>R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB</td></tr>
<tr><td rowspan="2">64-pin plastic TQFP (fine pitch) (7 × 7)</td><td>Mounted</td><td>R5F100LCAFC, R5F100LDAFC, R5F100LEAFC, R5F100LFAFC, R5F100LGAFC, R5F100LHAFC, R5F100LJAFC</td></tr>
<tr><td>Not mounted</td><td>R5F101LCAFC, R5F101LDAFC, R5F101LEAFC, R5F101LFAFC, R5F101LGAFC, R5F101LHAFC, R5F101LJAFC</td></tr>
<tr><td rowspan="2">64-pin plastic FBGA (4 × 4)</td><td>Mounted</td><td>R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG</td></tr>
<tr><td>Not mounted</td><td>R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG</td></tr>
</table>

Correct: (2/3)

Pin count	Package	Data flash	Part Number
(Omitted)			
64 pins	64-pin plastic LQFP (12x12)	Mounted	R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA, R5F100LKAFA, R5F100LLAFA
		Not mounted	R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA, R5F101LKAFA, R5F101LLAFA
	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB
		Not mounted	R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB
	64-pin plastic FBGA (4 × 4)	Mounted	R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG
		Not mounted	R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG

Pin configuration of 64-pin plastic TQFP (7 x 7) deleted (page 17)

Incorrect:

1.3.11 64-pin products

• 64-pin plastic LQFP (12 × 12)

• 64-pin plastic LQFP (fine pitch) (10 × 10)

• **64-pin plastic TQFP (fine pitch) (7 × 7)**

(Omitted)

Correct:

1.3.11 64-pin products

• 64-pin plastic LQFP (12 × 12)

• 64-pin plastic LQFP (fine pitch) (10 × 10)

(Omitted)

Package drawings of 64-pin plastic TQFP (7 x 7) deleted (page 1055)

Incorrect:

R5F100LCAFC, R5F100LDAFC, R5F100LEAFC, R5F100LFAFC, R5F100LGAFC, R5F100LHAFC, R5F100LJAFC

R5F101LCAFC, R5F101LDAFC, R5F101LEAFC, R5F101LFAFC, R5F101LGAFC, R5F101LHAFC, R5F101LJAFC

64-PIN PLASTIC TQFP (7x7)

Under development

Correct: Applicable page deleted

2. Incorrect descriptions of count registers in real-time clock deleted

Incorrect description of second count register (SEC) in real-time clock deleted (page 439)

Incorrect:

(5) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds.

It counts up when the sub-count register overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 59 to this register in BCD code. **If a value outside the range is set, the register value returns to the normal value after 1 period.**

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(5) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds.

It counts up when the sub-count register overflows. When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 59 to this register in BCD code.

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Incorrect description of minute count register (MIN) in real-time clock deleted (page 439)

Incorrect:

(6) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code. **If a value outside the range is set, the register value returns to the normal value after 1 period.**

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(6) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code.

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Incorrect description of hour count register (HOUR) in real-time clock deleted (page 440)

Incorrect:

(7) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0). If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system. **If a value outside the range is set, the register value returns to the normal value after 1 period.**

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Correct:

(7) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0). If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system.

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Incorrect description of day count register (DAY) in real-time clock deleted (page 442)

Incorrect:

(8) Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.

It counts up when the hour counter overflows.

This counter counts as follows.

(Omitted)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code. **If a value outside the range is set, the register value returns to the normal value after 1 period.**

The DAY register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Correct:

(8) Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.

It counts up when the hour counter overflows.

This counter counts as follows.

(Omitted)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code.

The DAY register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Incorrect description of week count register (WEEK) in real-time clock deleted (page 443)

Incorrect:

(9) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 06 to this register in BCD code. **If a value outside the range is set, the register value returns to the normal value after 1 period.**

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(9) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 06 to this register in BCD code.

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Incorrect description of month count register (MONTH) in real-time clock deleted (page 444)

Incorrect:

(10) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months.

It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code. **If a value outside the range is set, the register value returns to the normal value after 1 period.**

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Correct:

(10) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months.

It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code.

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Incorrect description of year count register (YEAR) in real-time clock deleted (page 444)

Incorrect:

(11) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, …, 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code. **If a value outside the range is set, the register value returns to the normal value after 1 period.**

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(11) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, …, 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code.

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

3. Caution of interval timer control register (ITMC) in 12-bit interval timer added (page 460)

Incorrect:

(3) Interval timer control register (ITMC)

(Omitted)

Cautions 1. Before changing the RINTE bit from 1 to 0, use the interrupt mask flag register to disable the INTIT interrupt servicing. When the operation starts (from 0 to 1) again, clear the ITIF flag, and then enable the interrupt servicing.

2. The value read from the RINTE bit is applied one count clock cycle after setting the RINTE bit.

3. Only change the setting of the ITCMP11 to ITCMP0 bits when RINTE = 0. However, it is possible to change the settings of the ITCMP11 to ITCMP0 bits at the same time as when changing RINTE from 0 to 1 or 1 to 0.

Correct:

(3) Interval timer control register (ITMC)

(Omitted)

Cautions 1. Before changing the RINTE bit from 1 to 0, use the interrupt mask flag register to disable the INTIT interrupt servicing. When the operation starts (from 0 to 1) again, clear the ITIF flag, and then enable the interrupt servicing.

2. The value read from the RINTE bit is applied one count clock cycle after setting the RINTE bit.

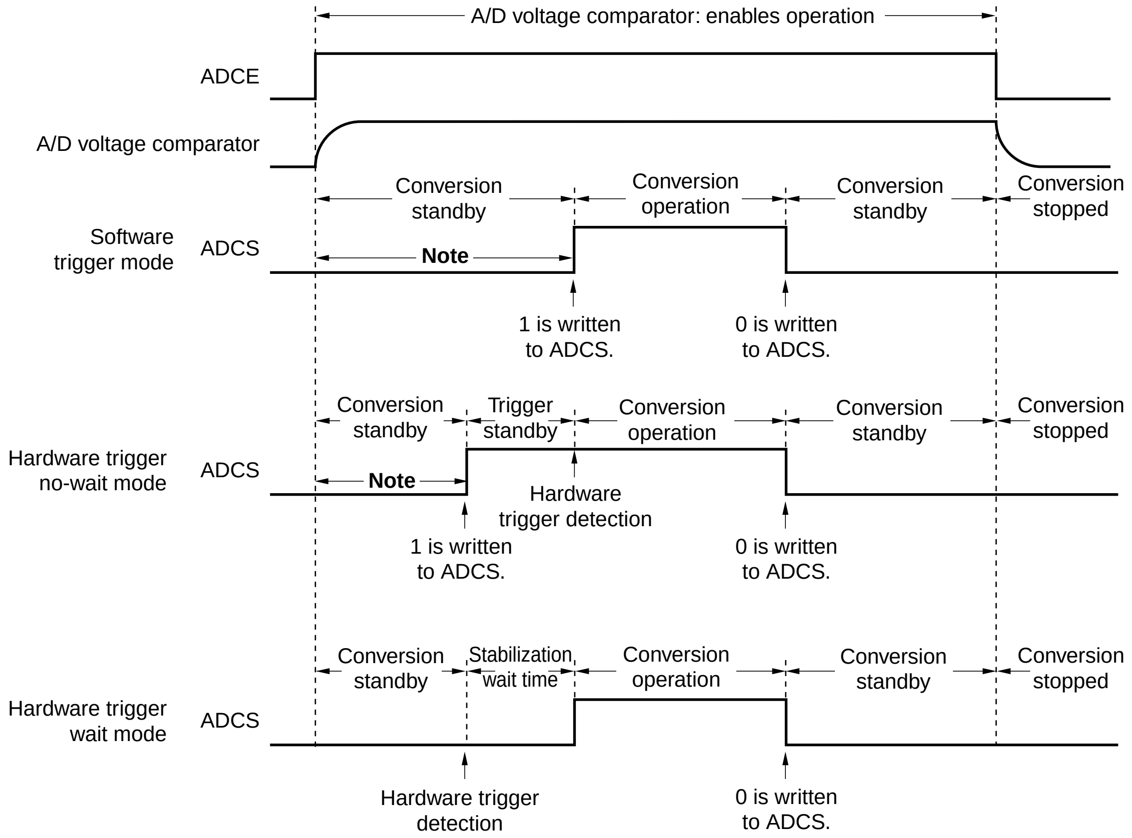
3. When setting the RINTE bit after returned from standby mode and entering standby mode again, confirm that the written value of the RINTE bit is reflected, or wait that more than one clock of the count clock has elapsed after returned from standby mode. Then enter standby mode.

4. Only change the setting of the ITCMP11 to ITCMP0 bits when RINTE = 0. However, it is possible to change the settings of the ITCMP11 to ITCMP0 bits at the same time as when changing RINTE from 0 to 1 or 1 to 0.

4. Added Explanations of timing chart when A/D voltage comparator is used (page 483)

Incorrect:

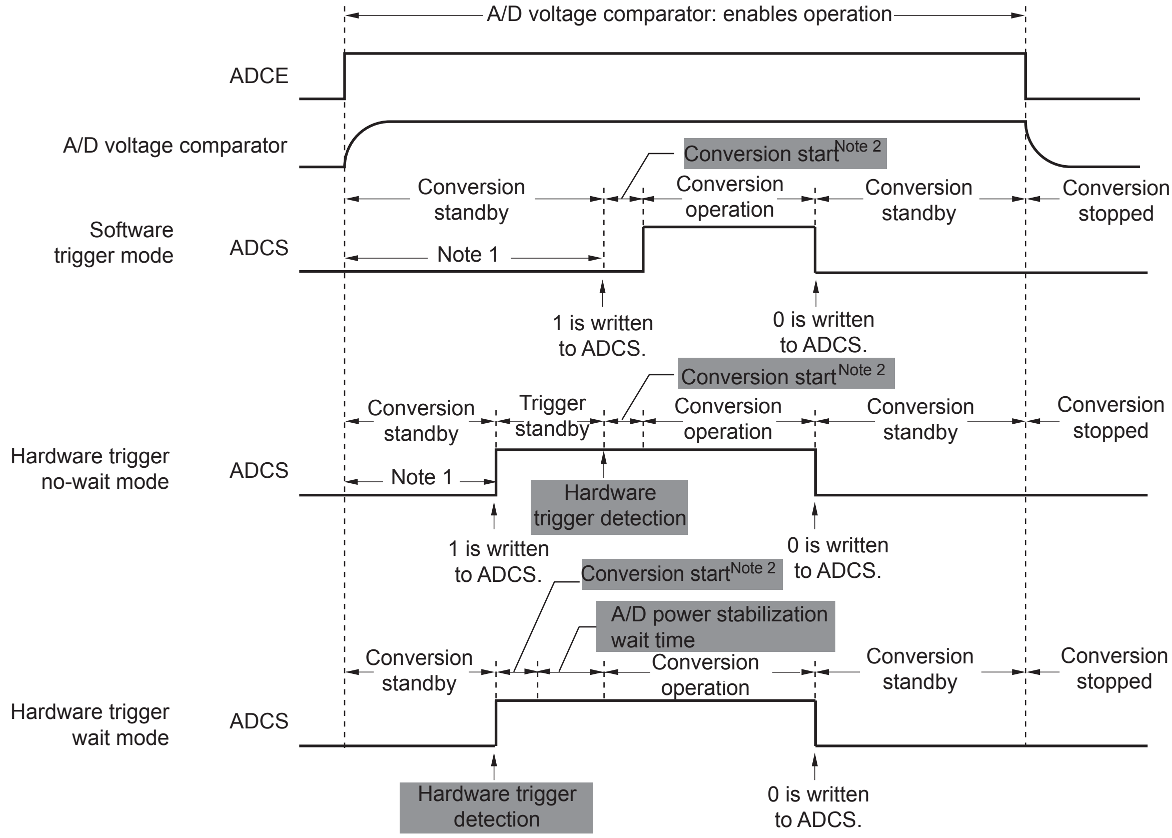
Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used



Note (Omitted)

Correct:

Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used



Note 1. (Omitted)

2. The following time is the maximum amount of time necessary to start conversion.

ADM0			Conversion Clock (f_{AD})	Conversion Start Time (Number of f_{CLK} Clocks)	
FR2	FR1	FR0		Software trigger mode/ Hardware trigger no wait mode	Hardware trigger wait mode
0	0	0	$f_{CLK}/64$	63	1
0	0	1	$f_{CLK}/32$	31	
0	1	0	$f_{CLK}/16$	15	
0	1	1	$f_{CLK}/8$	7	
1	0	0	$f_{CLK}/6$	5	
1	0	1	$f_{CLK}/5$	4	
1	1	0	$f_{CLK}/4$	3	
1	1	1	$f_{CLK}/2$	1	

Remark f_{CLK}: CPU/peripheral hardware clock frequency

5. Incorrect descriptions of Table 11-3 A/D Conversion Time Selection (6/8) to (8/8) when there is stabilization wait time (pages 489 to 491)

Incorrect:

Table 11-3. A/D Conversion Time Selection (6/8)

(6) 2.7 V ≤ VDD < 3.6 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (fAD)
FR2	FR1	FR0	LV1	LV0		fCLK = 1 MHz	fCLK = 2 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 µs	fCLK/64
0	0	1								54 µs	27 µs	fCLK/32
0	1	0							54 µs	27 µs	13.5 µs	fCLK/16
0	1	1						54 µs	27 µs	13.5 µs	6.75 µs	fCLK/8
1	0	0						40.5 µs	20.25 µs	10.125 µs	5.0625 µs	fCLK/6
1	0	1						33.75 µs	16.875 µs	8.4375 µs	Setting prohibited	fCLK/5
1	1	0					54 µs	27 µs	13.5 µs	6.75 µs		fCLK/4
1	1	1				54 µs	27 µs	13.5 µs	6.75 µs	Setting prohibited		fCLK/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	fCLK/64
0	0	1								50 µs	25 µs	fCLK/32
0	1	0							50 µs	25 µs	12.5 µs	fCLK/16
0	1	1						50 µs	25 µs	12.5 µs	6.25 µs	fCLK/8
1	0	0						37.5 µs	18.75 µs	9.375 µs	4.6875 µs	fCLK/6
1	0	1						31.25 µs	15.625 µs	7.8125 µs	Setting prohibited	fCLK/5
1	1	0					50 µs	25 µs	12.5 µs	6.25 µs		fCLK/4
1	1	1				50 µs	25 µs	12.5 µs	6.25 µs	Setting prohibited		fCLK/2
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 µs	fCLK/64
0	0	1								54 µs	27 µs	fCLK/32
0	1	0							54 µs	27 µs	Setting prohibited	fCLK/16
0	1	1						54 µs	27 µs	Setting prohibited		fCLK/8
1	0	0						40.5 µs	Setting prohibited			fCLK/6
1	0	1						33.75 µs				fCLK/5
1	1	0					54 µs	27 µs				fCLK/4
1	1	1				54 µs	27 µs	Setting prohibited				fCLK/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	fCLK/64
0	0	1								50 µs	25 µs	fCLK/32
0	1	0							50 µs	25 µs	Setting prohibited	fCLK/16
0	1	1						50 µs	25 µs	Setting prohibited		fCLK/8
1	0	0						37.5 µs	Setting prohibited			fCLK/6
1	0	1						31.25 µs				fCLK/5
1	1	0					50 µs	25 µs				fCLK/4
1	1	1				50 µs	25 µs	Setting prohibited				fCLK/2

Incorrect:

Table 11-3. A/D Conversion Time Selection (7/8)

(7) 1.8 V ≤ VDD < 2.7 V

When there is stabilization wait time (hardware trigger wait mode)

<table>
<tr><th colspan="5">A/D Converter Mode Register 0 (ADM0)</th><th rowspan="2">Mode</th><th colspan="6">Conversion Time Selection</th><th rowspan="2">Conversion Clock (fAD)</th></tr>
<tr><th>FR2</th><th>FR1</th><th>FR0</th><th>LV1</th><th>LV0</th><th>fCLK = 1 MHz</th><th>fCLK = 2 MHz</th><th>fCLK = 4 MHz</th><th>fCLK = 8 MHz</th><th>fCLK = 16 MHz (Note)</th><th>fCLK = 32 MHz</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="8">0</td><td rowspan="8">0</td><td rowspan="8">Normal 1</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td>fCLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>fCLK/32</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>fCLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>fCLK/8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>fCLK/6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>fCLK/5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>fCLK/4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>fCLK/2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="8">0</td><td rowspan="8">1</td><td rowspan="8">Normal 2</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td rowspan="8">Setting prohibited</td><td>fCLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>fCLK/32</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>fCLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>fCLK/8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>fCLK/6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>fCLK/5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>fCLK/4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>fCLK/2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="8">1</td><td rowspan="8">0</td><td rowspan="8">Low-Voltage 1</td><td rowspan="7">Setting prohibited</td><td rowspan="6">Setting prohibited</td><td rowspan="2">Setting prohibited</td><td rowspan="2">Setting prohibited</td><td>Setting prohibited</td><td>54 µs</td><td>fCLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>54 µs</td><td>27 µs</td><td>fCLK/32</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>54 µs</td><td>27 µs</td><td rowspan="6">Setting prohibited</td><td>fCLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>54 µs</td><td>27 µs</td><td rowspan="5">Setting prohibited</td><td>fCLK/8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>40.5 µs</td><td rowspan="4">Setting prohibited</td><td>fCLK/6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>33.75 µs</td><td>fCLK/5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>54 µs</td><td>27 µs</td><td>fCLK/4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>54 µs</td><td>27 µs</td><td>Setting prohibited</td><td>fCLK/2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="8">1</td><td rowspan="8">1</td><td rowspan="8">Low-Voltage 2</td><td rowspan="7">Setting prohibited</td><td rowspan="6">Setting prohibited</td><td rowspan="2">Setting prohibited</td><td rowspan="2">Setting prohibited</td><td>Setting prohibited</td><td>50 µs</td><td>fCLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>50 µs</td><td>25 µs</td><td>fCLK/32</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>50 µs</td><td>25 µs</td><td rowspan="6">Setting prohibited</td><td>fCLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>50 µs</td><td>25 µs</td><td rowspan="5">Setting prohibited</td><td>fCLK/8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>37.5 µs</td><td rowspan="4">Setting prohibited</td><td>fCLK/6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>31.25 µs</td><td>fCLK/5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>50 µs</td><td>25 µs</td><td>fCLK/4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>50 µs</td><td>25 µs</td><td>Setting prohibited</td><td>fCLK/2</td></tr>
</table>

Note (Omitted)

RENESAS

Incorrect:

Table 11-3. A/D Conversion Time Selection (8/8)

(8) 1.6 V ≤ V_{DD} < 1.8 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz (Note 2)	f_{CLK} = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/64
0	0	1	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/32
0	1	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/16
0	1	1	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/8
1	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/5
1	1	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/4
1	1	1	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/64
0	0	1	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/32
0	1	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/16
0	1	1	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/8
1	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/5
1	1	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/4
1	1	1	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/2
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**108 μs**	Setting prohibited	f_{CLK}/64
0	0	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	**108 μs**	Setting prohibited	Setting prohibited	f_{CLK}/32
0	1	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	**108 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/16
0	1	1	1	0	Low-Voltage 1	Setting prohibited	**108 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/8
1	0	0	1	0	Low-Voltage 1	Setting prohibited	**81 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1	1	0	Low-Voltage 1	**135 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/5
1	1	0	1	0	Low-Voltage 1	**108 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/4
1	1	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**100 μs**	Setting prohibited	f_{CLK}/64
0	0	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	**100 μs**	Setting prohibited	Setting prohibited	f_{CLK}/32
0	1	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	**100 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/16
0	1	1	1	1	Low-Voltage 2	Setting prohibited	**100 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/8
1	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1	1	1	Low-Voltage 2	**125 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/5
1	1	0	1	1	Low-Voltage 2	**100 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/4
1	1	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/2

Note (Omitted)

Correct:

Table 11-3. A/D Conversion Time Selection (6/8)

(6) 2.7 V ≤ V_{DD} < 3.6 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	f_{CLK}/64
0	0	1	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	f_{CLK}/32
0	1	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	27 μs	13.5 μs	f_{CLK}/16
0	1	1	0	0	Normal 1	Setting prohibited	Setting prohibited	54 μs	27 μs	13.5 μs	6.75 μs	f_{CLK}/8
1	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	40.5 μs	20.25 μs	10.125 μs	5.0625 μs	f_{CLK}/6
1	0	1	0	0	Normal 1	Setting prohibited	Setting prohibited	33.75 μs	16.875 μs	8.4375 μs	Setting prohibited	f_{CLK}/5
1	1	0	0	0	Normal 1	Setting prohibited	54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited	f_{CLK}/4
1	1	1	0	0	Normal 1	54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	f_{CLK}/64
0	0	1	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	f_{CLK}/32
0	1	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	25 μs	12.5 μs	f_{CLK}/16
0	1	1	0	1	Normal 2	Setting prohibited	Setting prohibited	50 μs	25 μs	12.5 μs	6.25 μs	f_{CLK}/8
1	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	37.5 μs	18.75 μs	9.375 μs	4.6875 μs	f_{CLK}/6
1	0	1	0	1	Normal 2	Setting prohibited	Setting prohibited	31.25 μs	15.625 μs	7.8125 μs	Setting prohibited	f_{CLK}/5
1	1	0	0	1	Normal 2	Setting prohibited	50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited	f_{CLK}/4
1	1	1	0	1	Normal 2	50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited	Setting prohibited	f_{CLK}/2
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**42 μs**	f_{CLK}/64
0	0	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**42 μs**	**21 μs**	f_{CLK}/32
0	1	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	**42 μs**	**21 μs**	Setting prohibited	f_{CLK}/16
0	1	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	**42 μs**	**21 μs**	Setting prohibited	Setting prohibited	f_{CLK}/8
1	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	**31.5 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	**26.25 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/5
1	1	0	1	0	Low-Voltage 1	Setting prohibited	**42 μs**	**21 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/4
1	1	1	1	0	Low-Voltage 1	**42 μs**	**21 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**38 μs**	f_{CLK}/64
0	0	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**38 μs**	**19 μs**	f_{CLK}/32
0	1	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	**38 μs**	**19 μs**	Setting prohibited	f_{CLK}/16
0	1	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	**38 μs**	**19 μs**	Setting prohibited	Setting prohibited	f_{CLK}/8
1	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	**28.5 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/6
1	0	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	**23.75μs**	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/5
1	1	0	1	1	Low-Voltage 2	Setting prohibited	**38 μs**	**19 μs**	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/4
1	1	1	1	1	Low-Voltage 2	**38 μs**	**19 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f_{CLK}/2

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Correct:

Table 11-3. A/D Conversion Time Selection (7/8)

(7) 1.8 V ≤ V_{DD} < 2.7 V

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						on Clock
FR2	FR1	FR0	LV1	LV0		fCLK = 1 MHz	fCLK = 2 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz[Note]	fCLK = 32 MHz	
x	x	x	0	0	Normal 1	Setting prohibited						–
x	x	x	0	1	Normal 2	Setting prohibited						–
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**42 μs**	fCLK/64
0	0	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**42 μs**	**21 μs**	fCLK/32
0	1	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	**42 μs**	**21 μs**	Setting prohibited	fCLK/16
0	1	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	**42 μs**	**21 μs**	Setting prohibited	Setting prohibited	fCLK/8
1	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	**31.5 μs**	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/6
1	0	1	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	**26.25 μs**	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/5
1	1	0	1	0	Low-Voltage 1	Setting prohibited	**42 μs**	**21 μs**	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/4
1	1	1	1	0	Low-Voltage 1	**42 μs**	**21 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	38 μs	fCLK/64
0	0	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**38 μs**	**19 μs**	fCLK/32
0	1	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	**38 μs**	**19 μs**	Setting prohibited	fCLK/16
0	1	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	**38 μs**	**19 μs**	Setting prohibited	Setting prohibited	fCLK/8
1	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	**28.5 μs**	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/6
1	0	1	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	**28.75 μs**	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/5
1	1	0	1	1	Low-Voltage 2	Setting prohibited	**38 μs**	**19 μs**	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/4
1	1	1	1	1	Low-Voltage 2	**38 μs**	**19 μs**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/2

Note (Omitted)

Correct:

Table 11-3. A/D Conversion Time Selection (8/8)

(8) 1.6 V ≤ VDD < 1.8 V

When there is stabilization wait time (hardware trigger wait mode)

<table>
<tr><th colspan="5">A/D Converter Mode Register 0 (ADM0)</th><th rowspan="2">Mode</th><th colspan="6">Conversion Time Selection</th><th rowspan="2">Conversion Clock (fAD)</th></tr>
<tr><th>FR2</th><th>FR1</th><th>FR0</th><th>LV1</th><th>LV0</th><th>fCLK = 1 MHz</th><th>fCLK = 2 MHz</th><th>fCLK = 4 MHz</th><th>fCLK = 8 MHz</th><th>fCLK = 16 MHz Note 2</th><th>fCLK = 32 MHz</th></tr>
<tr><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>Normal 1</td><td>Setting prohibited</td><td>_</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td></tr>
<tr><td>x</td><td>x</td><td>x</td><td>0</td><td>1</td><td>Normal 2</td><td>Setting prohibited</td><td>_</td><td>x</td><td>x</td><td>x</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="8">1</td><td rowspan="8">0</td><td rowspan="8">Low-Voltage 1</td><td rowspan="5">Setting prohibited</td><td rowspan="3">Setting prohibited</td><td rowspan="2">Setting prohibited</td><td>Setting prohibited</td><td>**84 μs**</td><td rowspan="8">Setting prohibited</td><td>fCLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>**84 μs**</td><td rowspan="7">Setting prohibited</td><td>fCLK/32</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>**84 μs**</td><td rowspan="6">Setting prohibited</td><td>fCLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>**84 μs**</td><td rowspan="5">Setting prohibited</td><td>fCLK/8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>**63 μs**</td><td>fCLK/6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>**105 μs**</td><td rowspan="3">Setting prohibited</td><td>fCLK/5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>**84 μs**</td><td>fCLK/4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td><td>fCLK/2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="8">1</td><td rowspan="8">1</td><td rowspan="8">Low-Voltage 2</td><td rowspan="5">Setting prohibited</td><td rowspan="3">Setting prohibited</td><td rowspan="2">Setting prohibited</td><td>Setting prohibited</td><td>**76 μs**</td><td rowspan="8">Setting prohibited</td><td>fCLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>**76 μs**</td><td rowspan="7">Setting prohibited</td><td>fCLK/32</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>**76 μs**</td><td rowspan="6">Setting prohibited</td><td>fCLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>**76 μs**</td><td rowspan="5">Setting prohibited</td><td>fCLK/8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td rowspan="4">Setting prohibited</td><td>fCLK/6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>**95 μs**</td><td>fCLK/5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>**76 μs**</td><td>fCLK/4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td><td>fCLK/2</td></tr>
</table>

Note (Omitted)

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6. Note when entering A/D converter standby mode added

Note on A/D converter mode register 2 (ADM2) added (page 493)

Incorrect:

(4) A/D converter mode register 2 (ADM2)

(Omitted)

Caution Only rewrite the value of the ADM2 register while conversion operation is stopped (which is indicated by the ADCS bit of A/D converter mode register 0 (ADM0) being 0).

Correct:

(4) A/D converter mode register 2 (ADM2)

(Omitted)

Cautions 1. Only rewrite the value of the ADM2 register while conversion operation is stopped (which is indicated by the ADCS bit of A/D converter mode register 0 (ADM0) being 0).

2. When entering STOP mode or HALT mode while the CPU is operating on the subsystem clock, do not set ADREFP1 to 1. When selecting internal reference voltage (ADREFP1, ADREFP0 = 1, 0), the current value of A/D converter reference voltage current (I_{ADREF}) shown in 29.4.2 Supply current characteristics is added.

Note on analog input channel specification register (ADS) added (page 497)

Incorrect:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (2/2)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

(Omitted)

Cautions 1. Be sure to clear bits 5 and 6 to 0.

(Omitted)

6. If using AVREFP as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.
7. If using AVREFM as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.
8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source.

Correct:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (2/2)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

(Omitted)

Cautions 1. Be sure to clear bits 5 and 6 to 0.

(Omitted)

6. If using AVREFP as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.
7. If using AVREFM as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.
8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source.
9. When entering STOP mode or HALT mode while the CPU is operating on the subsystem clock, do not set ADISS to 1. When setting ADISS to 1, the current value of the A/D converter reference voltage current (I_{ADREF}) shown in 29.4.2 Supply current characteristics is added.

7. Incorrect descriptions of maskable interrupt request acknowledgement operation revised

Revised incorrect description of time from generation of maskable interrupt until servicing in Table 16-4. (page 842)

Incorrect:

16.4.1 Maskable interrupt request acknowledgment

(Omitted)

Table 16.4 Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time Note
Servicing time	9 clocks	**14 clocks**

Note If an interrupt request is generated just before the RET instruction, the wait time becomes longer.

Remark 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

Correct:

16.4.1 Maskable interrupt request acknowledgment

(Omitted)

Table 16.4 Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time Note
Servicing time	9 clocks	16 clocks

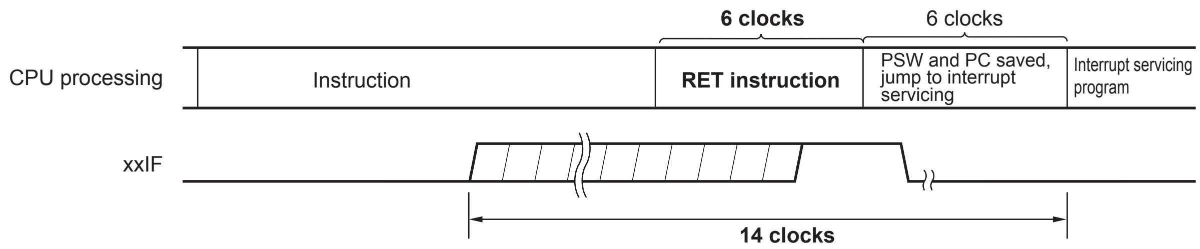
Note Maximum time does not apply when an instruction from the internal RAM area is executed.

Remark 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

Figure 16-9. Incorrect description of interrupt request acknowledgment timing (maximum time) revised (page 844)

Incorrect:

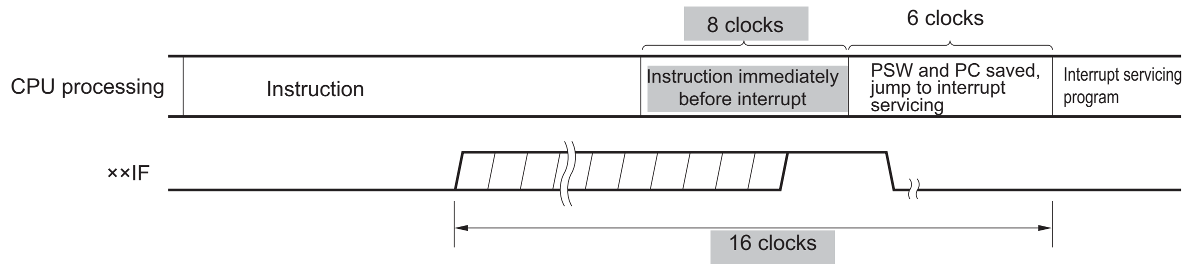
Figure 16-9. Interrupt Request Acknowledgment Timing (Maximum Time)



Remark 1 clock: 1/fCLK (fCLK: CPU clock)

Correct:

Figure 16-9. Interrupt Request Acknowledgment Timing (Maximum Time)



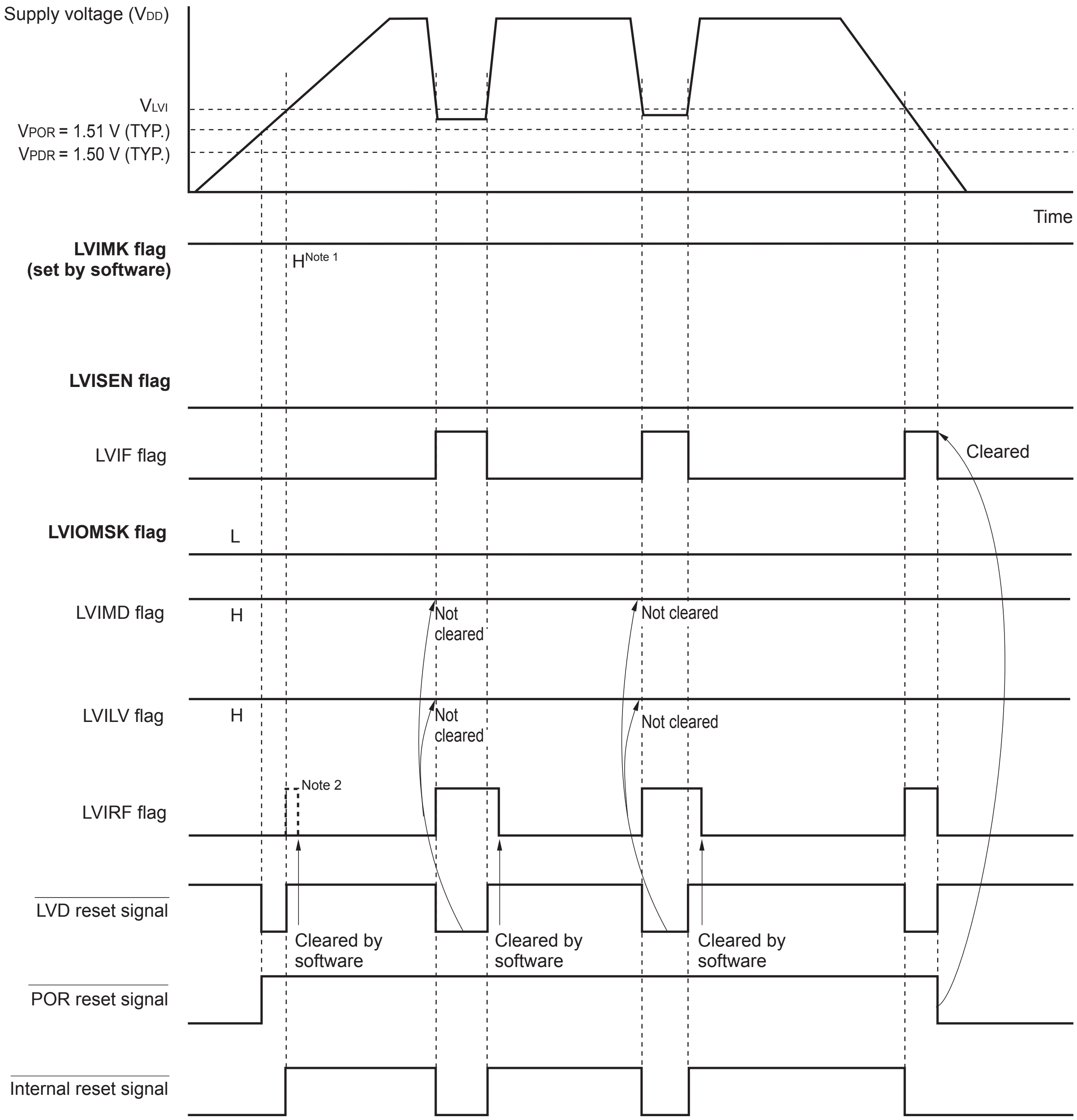
Remark 1 clock: 1/fCLK (fCLK: CPU clock)

8. Incorrect descriptions of voltage detector (LVD) timing chart revised

Figure 21-4. Incorrect descriptions of timing of voltage detector internal reset signal generation revised (page 894)

Incorrect:

Figure 21-4. Timing of Voltage Detector Internal Reset Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. LVIRF flag is bit 0 of the reset control flag register (RESF).

The LVIRF flag may become 1 from the beginning due to the power-on waveform.

For details of the RESF register, see CHAPTER 19 RESET FUNCTION.

Correct:

Figure 21-4. Timing of Voltage Detector Internal Reset Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 1)

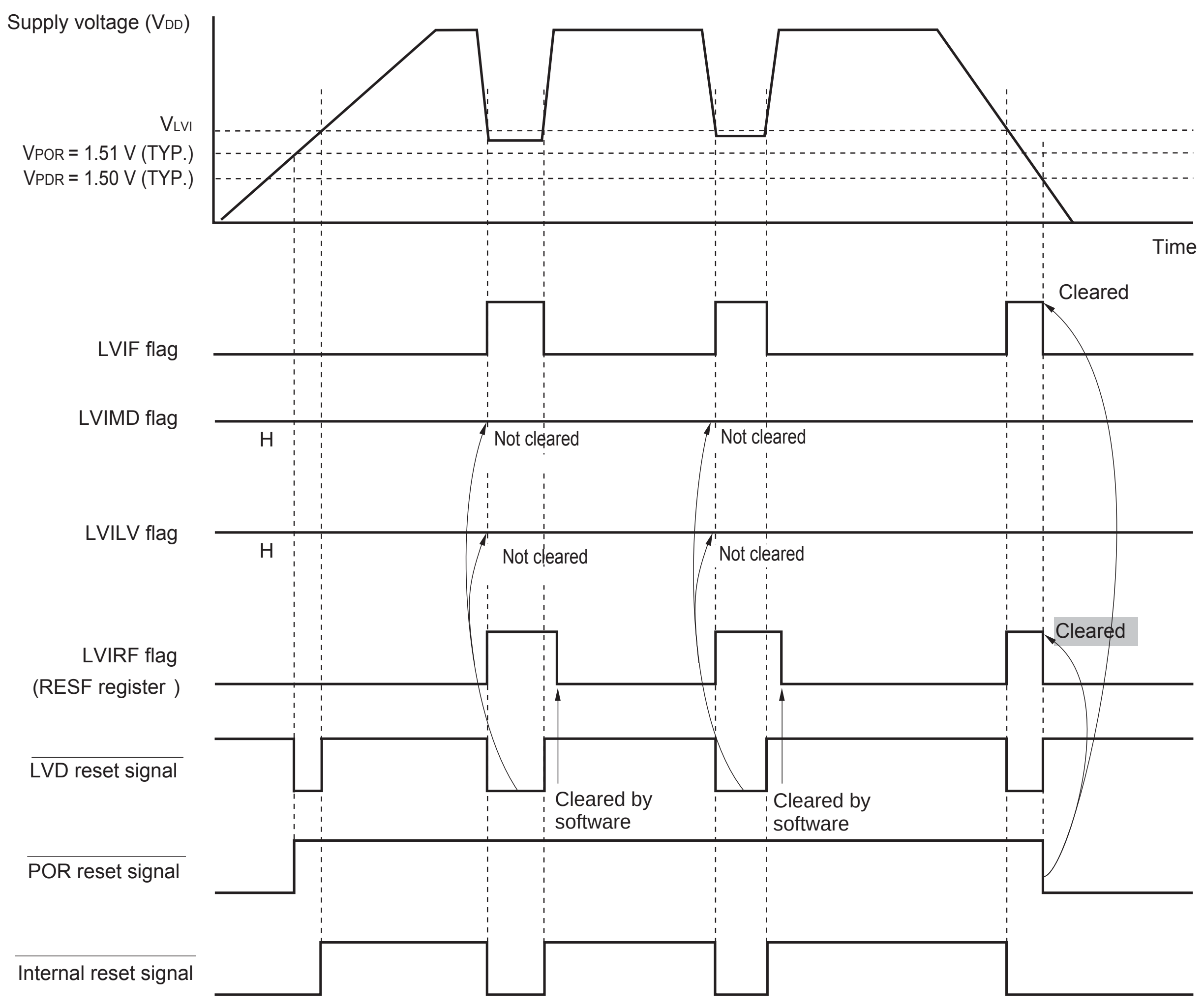
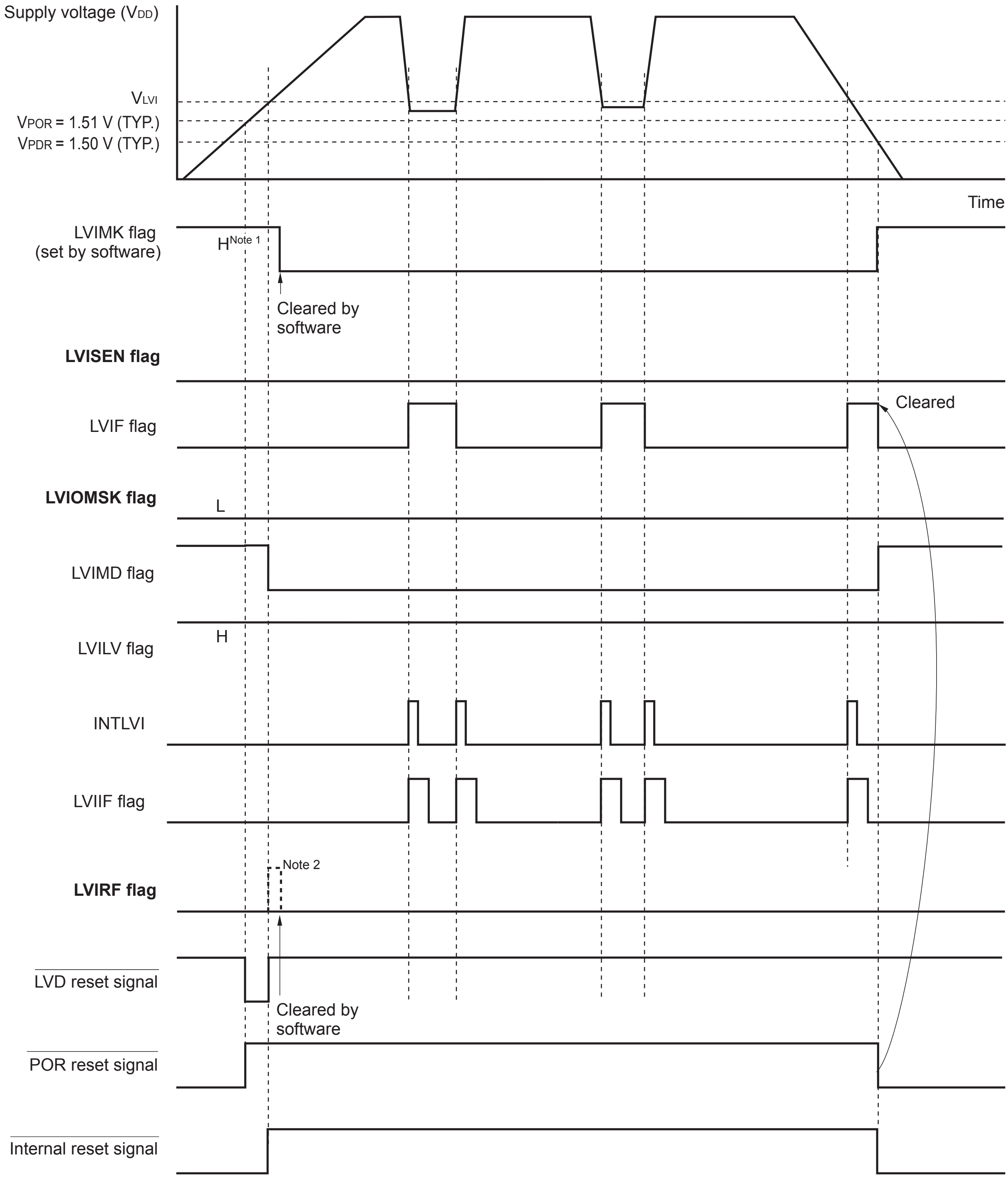


Figure 21-5. Incorrect description of voltage detector internal interrupt signal generation timing revised (page 896)

Incorrect:

Figure 21-5. Timing of Voltage Detector Internal Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 0, 1)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. LVIRF flag is bit 0 of the reset control flag register (RESF).

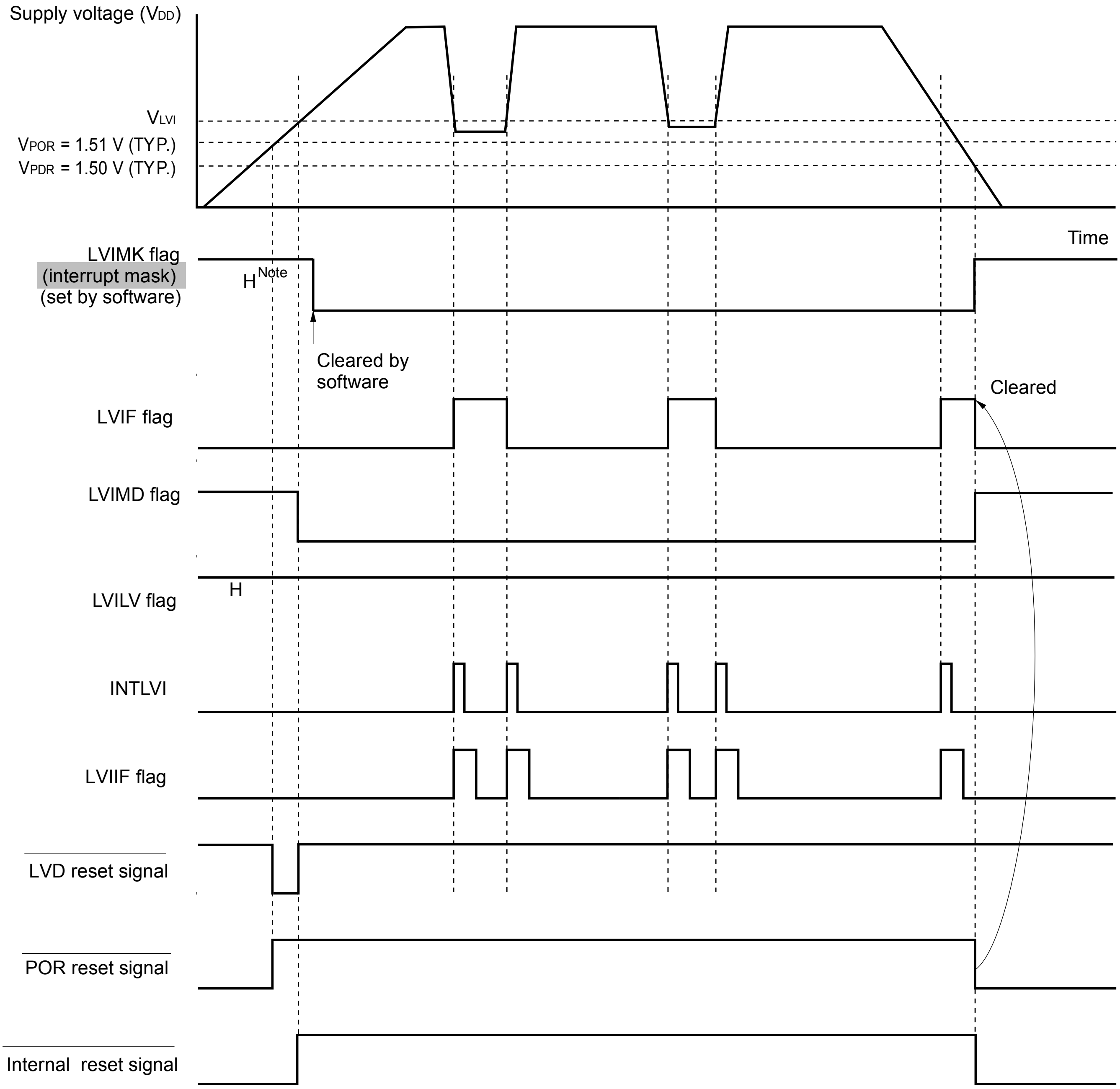
The LVIRF flag may become 1 from the beginning due to the power-on waveform.

For details of the RESF register, see CHAPTER 19 RESET FUNCTION.

Correct:

Figure 21-5. Timing of Voltage Detector Internal Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 0, 1)



Note The LVIMK flag is set to “1” by reset signal generation.

9. Incorrect description of voltage detector (LVD) interrupt and reset mode revised

Incorrect description of when used as interrupt and reset mode revised (page 897)

Incorrect:

21.4.3 When used as interrupt and reset mode

- When starting operation

Specify the operation mode (the interrupt and reset (LVIMDS1, LVIMDS0 = 1, 0)) and the detection voltage (V_{LVIH}, V_{LVIL}) by using the option byte 000C1H/010C1H.

(Omitted)

Figure 21-6 shows the timing of the internal reset signal and interrupt signal generated by the voltage detector.

Caution The LVIRF flag may become 1 from the beginning due to the power-on waveform.

For details of the RESF register, see CHAPTER 19 RESET FUNCTION.

Correct:

21.4.3 When used as interrupt and reset mode

- When starting operation

Specify the operation mode (the interrupt and reset (LVIMDS1, LVIMDS0 = 1, 0)) and the detection voltage (V_{LVIH}, V_{LVIL}) by using the option byte 000C1H/010C1H.

(Omitted)

Figures 21-6 shows the timing of voltage detector reset signal and interrupt signal generation.

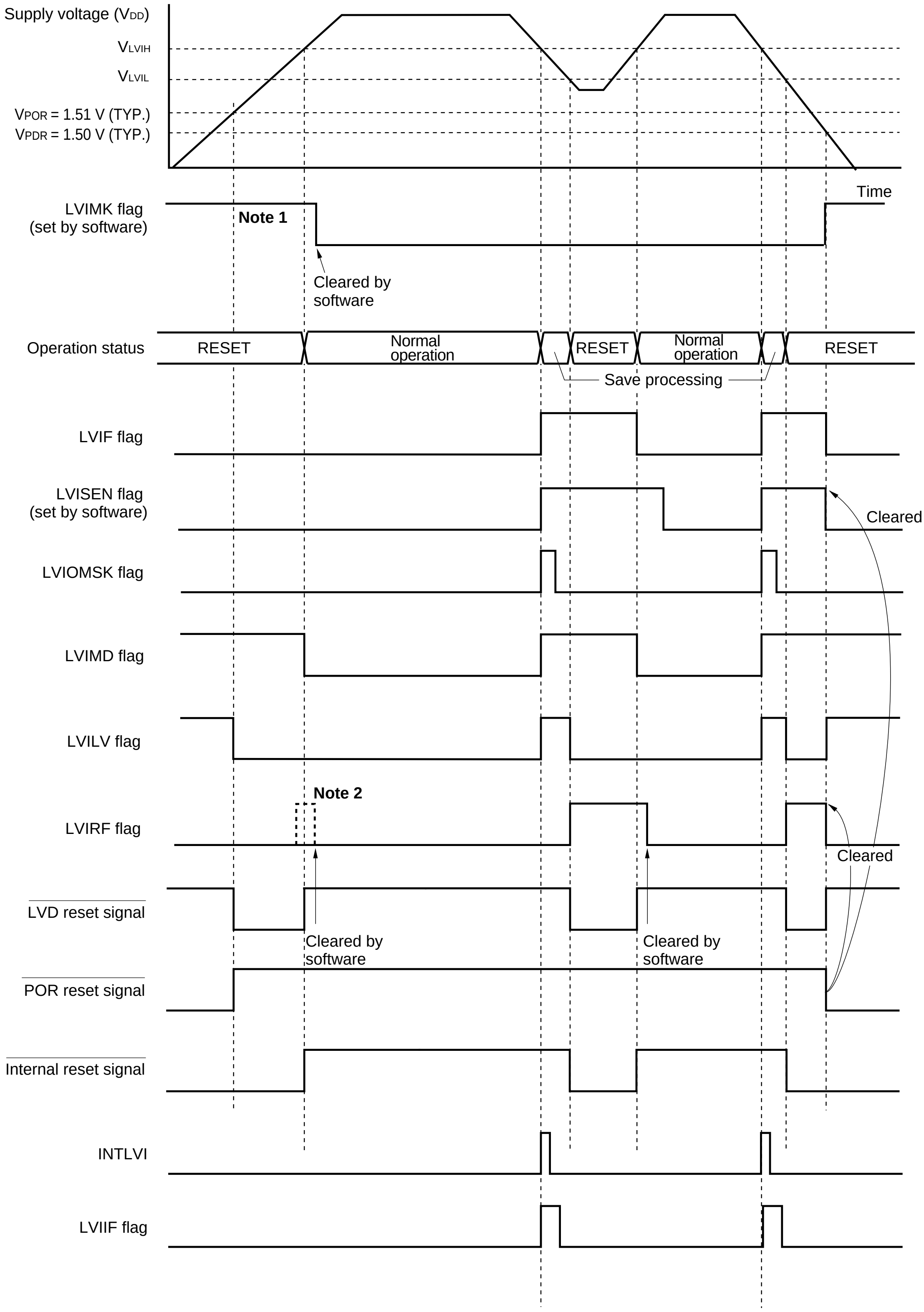
Perform the processing according to figure 21-7 Processing procedure after an interrupt is generated and figure 21-8 Initial setting of interrupt and reset mode.

Incorrect description of timing of voltage detector reset signal and interrupt signal generation revised (page 898)

Incorrect:

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 1, 0)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. LVIRF flag is bit 0 of the reset control flag register (RESF). The LVIRF flag may become 1 from the beginning due to the power-on waveform. For details of the RESF register, see CHAPTER 19 RESET FUNCTION.

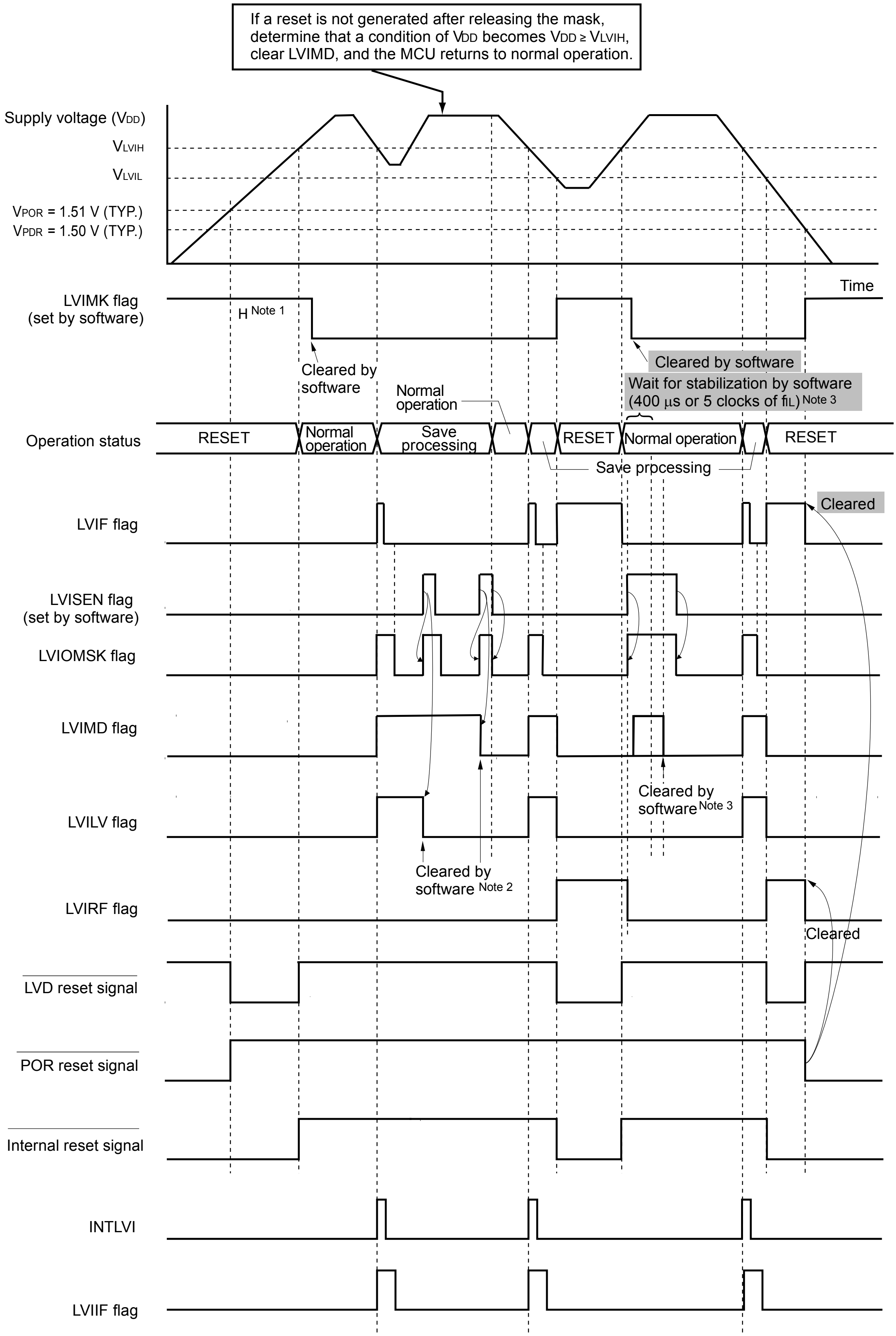
Remark V_{POR}: POR power supply rise detection voltage

V_{PDR}: POR power supply fall detection voltage

Correct:

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (1/2)



RENESAS

Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. After an interrupt is generated, perform the processing according to figure 21-7 Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.

3. After a reset is released, perform the processing according to figure 21-8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode.

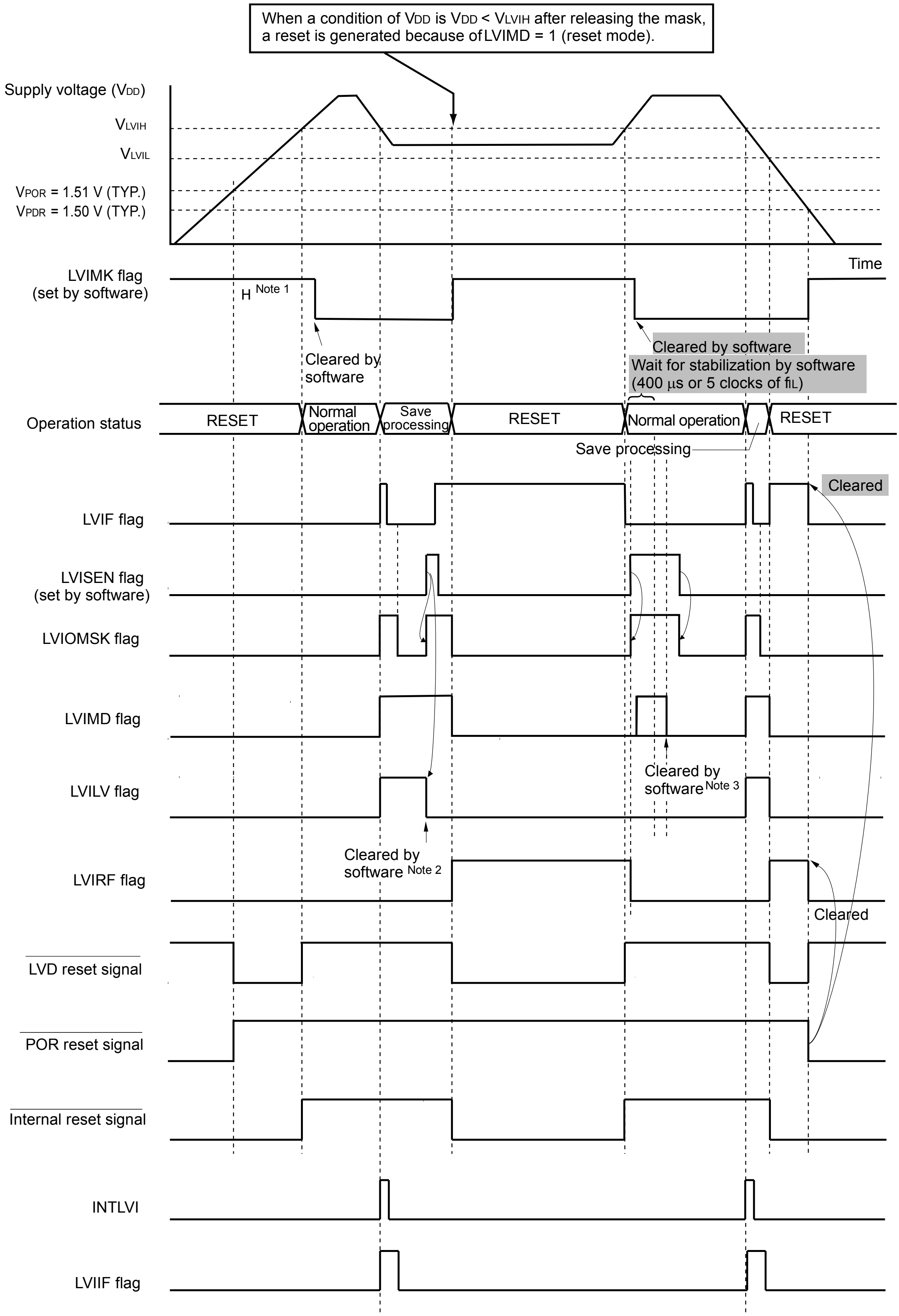
Remark V_{POR}: POR power supply rise detection voltage

V_{PDR}: POR power supply fall detection voltage

Correct:

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (2/2)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. After an interrupt is generated, perform the processing according to figure 21-7 Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.

3. After a reset is released, perform the processing according to figure 21-8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode.

Remark V_{POR}: POR power supply rise detection voltage

V_{PDR}: POR power supply fall detection voltage

Figure 21-7. Processing Procedure After an Interrupt Is Generated

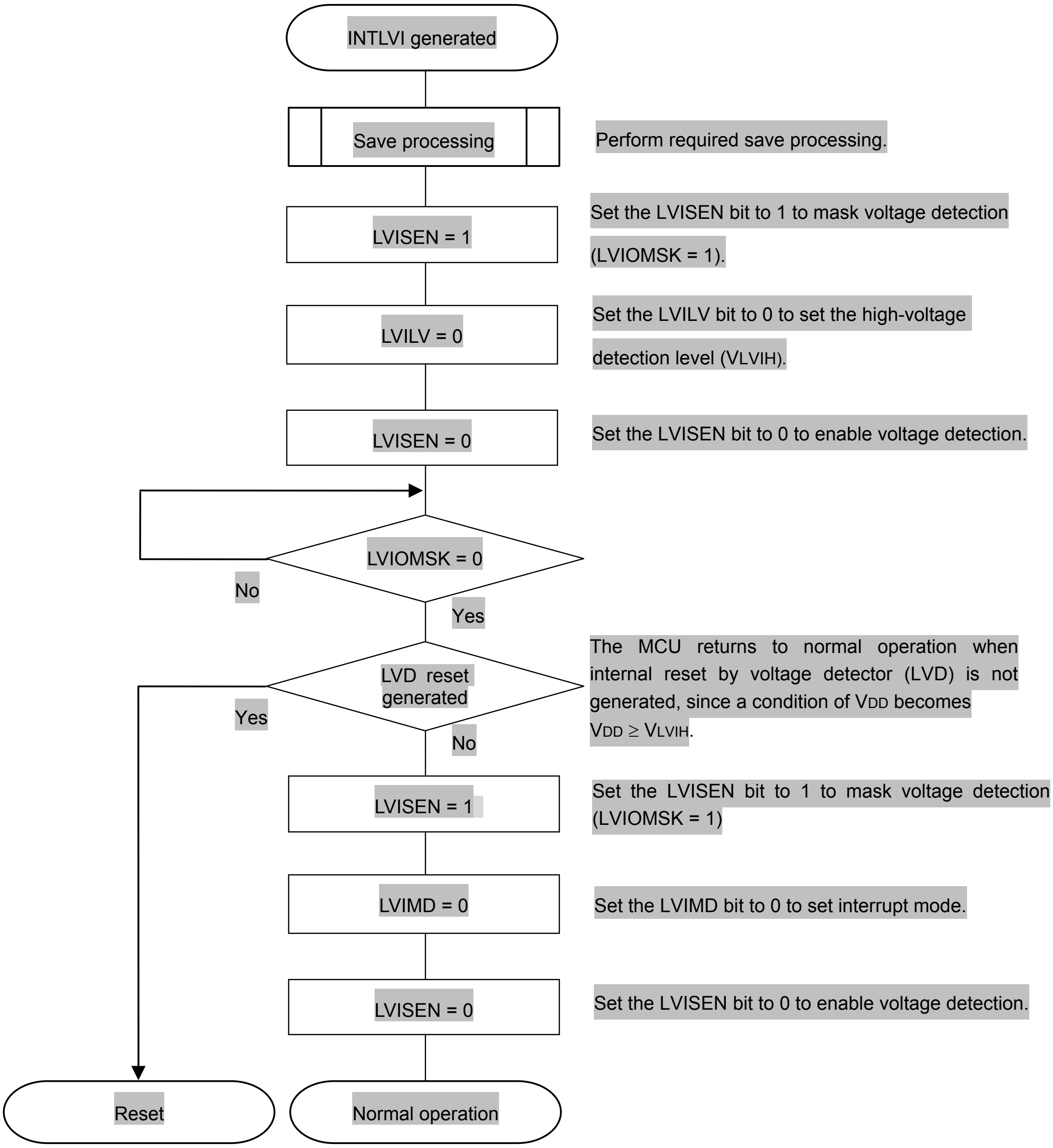
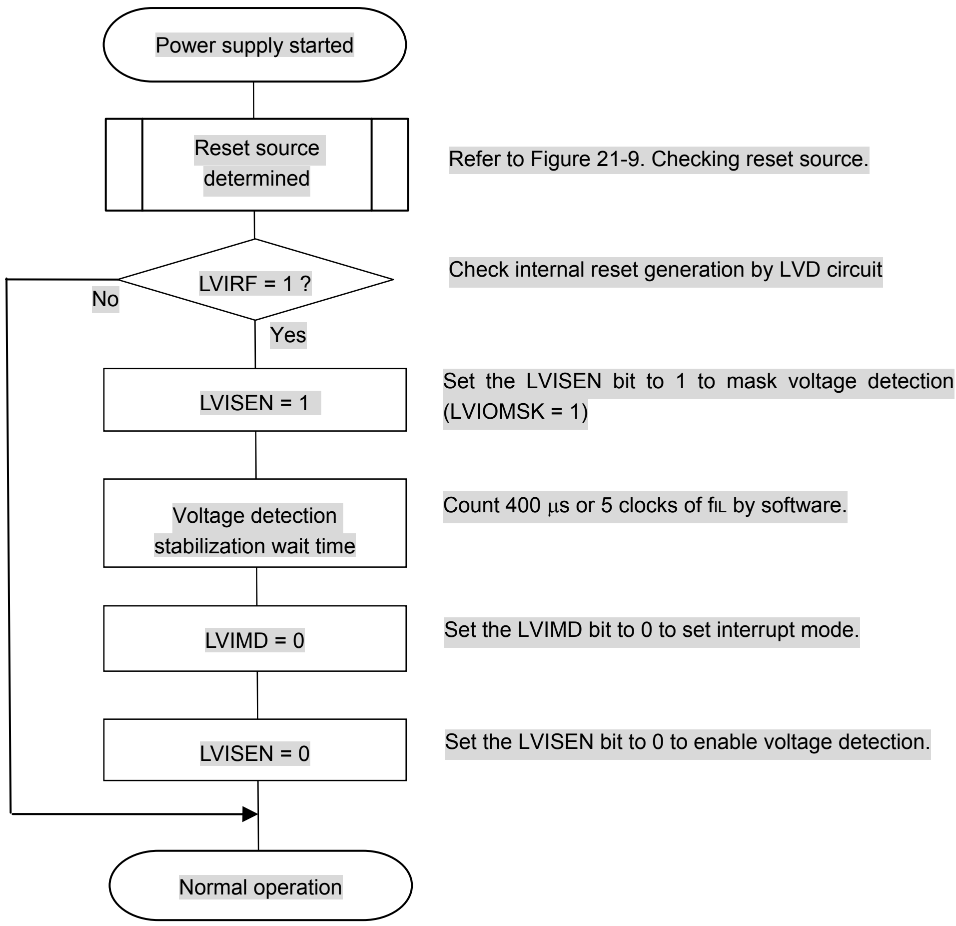


Figure 21-8. Explanations of initial setting of interrupt and reset mode added (page 899)

When setting an interrupt and reset mode (LVIMDS1, LVIMDS0 = 1, 0), voltage detection stabilization wait time for 400 μs or 5 clocks of f_{IL} is necessary after LVD reset is released (LVIRF = 1). After waiting until voltage detection stabilizes, (0) clear the LVIMD bit for initialization. While voltage detection stabilization wait time is being counted and when the LVIMD bit is rewritten, set LVISEN to 1 to mask a reset or interrupt generation by LVD.

Figure 21-8. shows the procedure for initial setting of interrupt and reset mode.

Figure 21-8. Initial Setting of Interrupt and Reset Mode



Remark f_{IL}: Low-speed on-chip oscillator clock frequency

10. Added common item for all RL78/G13 products in 29.4.2 Supply current characteristics of Electrical specifications (page 1005)

Incorrect:

(4) Common to RL78/G13 all products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz	Real-time clock operation		0.02		μA
			Interval timer operation		0.02		
Watchdog timer operating current	I_{WDT} Notes 2,3	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 4	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
Temperature sensor operating current	I_{TMPS}				75		μA
LVD operating current	I_{LVI} Notes 5				0.08		μA
BGO operating current	I_{BGO} Notes 6				2.50	12.20	mA

Note (Omitted)

Correct:

(4) Common to RL78/G13 all products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz	Real-time clock operation		0.02		μA
			Interval timer operation		0.02		
Watchdog timer operating current	I_{WDT} Notes 2,3	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 4	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF}				75		μA
Temperature sensor operating current	I_{TMPS}				75		μA
LVD operating current	I_{LVI} Notes 5				0.08		μA
BGO operating current	I_{BGO} Notes 6				2.50	12.20	mA

Note (Omitted)

11. Explanations when using temperature sensor and internal reference voltage (1.45 V) of A/D converter added

Explanation of Figure 11-7. A/D converter mode register 2 (ADM2) added (page 493)

Incorrect:

Figure 11-7. Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	1	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	**Supplied from the internal reference voltage (1.45 V)**
1	1	Setting prohibited
(Omitted)		

(Omitted)

Correct:

Figure 11-7. Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	1	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage (1.45 V)[Note]
1	1	Setting prohibited
(Omitted)		

Note This setting value can be selected only in HS (high-speed main) mode.

(Omitted)

Explanation of Figure 11-11. Analog input channel specification register (ADS) added (page 496)

Incorrect:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (1/2)

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV_{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
(Omitted)							
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	–	**Temperature sensor output**
1	0	0	0	0	1	–	**Internal reference voltage output (1.45 V)**
Other than the above						Setting prohibited	

Notes 1. 20-, 24-, 25-, 30-, 32-pin products: P01/ANI16 pin

2. 20-, 24-, 25-, 30-, 32-pin products: P00/ANI17 pin

Correct:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (1/2)

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV_{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
(Omitted)							
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output[Note 3]
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V)[Note 3]
Other than the above						Setting prohibited	

Notes 1. 20-, 24-, 25-, 30-, 32-pin products: P01/ANI16 pin

2. 20-, 24-, 25-, 30-, 32-pin products: P00/ANI17 pin

3. This setting value can be selected only in HS (high-speed main) mode.

Explanation of 11.7.4 Setup when using temperature sensor added (page 523)

Incorrect:

11.7.4 Setup when using temperature sensor (example for software trigger mode and one-shot conversion mode)

Figure 11-35. Setup When Using Temperature Sensor

(Omitted)

Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

Correct:

11.7.4 Setup when using temperature sensor (example for software trigger mode and one-shot conversion mode)

Figure 11-35. Setup When Using Temperature Sensor

(Omitted)

Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

Caution This setting can be used only in HS (high-speed main) mode.

Explanation of (2) Input range of ANI0 to ANI14 and ANI16 to ANI26 pins in 11.10 Cautions for A/D Converter added (page 530)

Incorrect:

11.10 Cautions for A/D Converter

(2) Input range of ANI0 to ANI14 and ANI16 to ANI26 pins

Observe the rated range of the ANI0 to ANI14 and ANI16 to ANI26 pins input voltage. If a voltage of V_{DD} and AV_{REFP} or higher and V_{SS} and AV_{REFM} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage (1.45 V) is selected reference voltage source for the + side of the A/D converter, do not input internal reference voltage or higher voltage to a pin selected by the ADS register. However, it is no problem that a pin not selected by the ADS register is inputed voltage greater than the internal reference voltage.

Correct:

11.10 Cautions for A/D Converter

(2) Input range of ANI0 to ANI14 and ANI16 to ANI26 pins

Observe the rated range of the ANI0 to ANI14 and ANI16 to ANI26 pins input voltage. If a voltage of V_{DD} and AV_{REFP} or higher and V_{SS} and AV_{REFM} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage (1.45 V) is selected reference voltage source for the + side of the A/D converter, do not input internal reference voltage or higher voltage to a pin selected by the ADS register. However, it is no problem that a pin not selected by the ADS register is inputed voltage greater than the internal reference voltage.

Caution The internal reference voltage (1.45 V) can be selected only in HS (high-speed main) mode.

12. Explanations of A/D test function in Safety functions chapter (section 22.3.8) added

Explanation of Figure 22-15. A/D test register (ADTES) added (page 917)

Incorrect:

(1) A/D test register (ADTES)

Figure 22-15. Format of A/D Test Register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

ADTES1	ADTES0	A/D conversion target
0	0	ANIxx (This is specified using the analog input channel specification register (ADS).)
1	0	AV_{REFM}
1	1	AV_{REFP}
Other than the above		Setting prohibited

Correct:

(1) A/D test register (ADTES)

Figure 22-15. Format of A/D Test Register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

ADTES1	ADTES0	A/D conversion target
0	0	ANIxx (This is specified using the analog input channel specification register (ADS).)Note
1	0	AV_{REFM}
1	1	AV_{REFP}
Other than the above		Setting prohibited

Note The temperature sensor output and internal reference voltage output (1.45 V) can be selected only in HS (high-speed main) mode.

Explanation of Figure 22-16. Analog input channel specification register (ADS) added (pages 918 to 919)

Incorrect:

Figure 22-16. Format of Analog Input Channel Specification Register (ADS) (1/2)

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV_{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
(Omitted)							
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	–	**Temperature sensor output**
1	0	0	0	0	1	–	**Internal reference voltage output (1.45 V)**
Other than the above						Setting prohibited	

(Notes and cautions are listed on the next page.)

Notes 1. 20-, 24-, 25-, 30-, 32-pin products: P01/ANI16 pin

2. 20-, 24-, 25-, 30-, 32-pin products: P00/ANI17 pin

(Omitted)

Correct:

Figure 22-16. Format of Analog Input Channel Specification Register (ADS) (1/2)

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV_{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
(Omitted)							
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output[Note 3]
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V)[Note 3]
Other than the above						Setting prohibited	

(Notes and cautions are listed on the next page.)

Notes 1. 20-, 24-, 25-, 30-, 32-pin products: P01/ANI16 pin

2. 20-, 24-, 25-, 30-, 32-pin products: P00/ANI17 pin

3. This setting value can be selected only in HS (high-speed main) mode.

(Omitted)

13. Conditions of A/D converter characteristics in Electrical specifications chapter (section 29.7.1) added

Condition of (1) When AVREF (+) = AVREFP/ANI0, AVREF (–) = AVREFM/ANI1, target ANI pin : ANI2 to ANI14 added (page 1032)

Incorrect:

(1) When $AV_{REF\,(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF\,(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI2 to ANI14

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Notes 1, 2]	AINL	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	(Omitted)					
Zero-scale error[Notes 1, 2]	EZS						
Full-scale error[Notes 1, 2]	EFS						
Integral linearity error[Note 1]	ILE						
Differential linearity error[Note 1]	DLE						
Reference voltage (+)	AV_{REFP}			1.6		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
	V_{BGR}	**2.4 V ≤ V_{DD} ≤ 5.5 V**		1.38	1.45	1.5	V

(Omitted)

Correct:

(1) When $AV_{REF\,(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF\,(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI2 to ANI14

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Notes 1, 2]	AINL	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	(Omitted)					
Zero-scale error[Notes 1, 2]	EZS						
Full-scale error[Notes 1, 2]	EFS						
Integral linearity error[Note 1]	ILE						
Differential linearity error [Note 1]	DLE						
Reference voltage (+)	AV_{REFP}			1.6		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
	V_{BGR}	2.4 V ≤ V_{DD} ≤ 5.5 V	HS mode	1.38	1.45	1.5	V

(Omitted)

Condition of (2) When AVREF (+) = AVREFP/ANI0, AVREF (–) = AVREFM/ANI1, target ANI pin : ANI16 to ANI26 added (page 1033)

Incorrect:

(2) When $AV_{REF\,(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF\,(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI16 to ANI26

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Notes 1, 2]	AINL	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±8.5	LSB
Conversion time	t_{CONV}	(Omitted)					
Zero-scale error[Notes 1, 2]	EZS						
Full-scale error[Notes 1, 2]	EFS						
Integral linearity error[Note 1]	ILE						
Differential linearity error[Note 1]	DLE						
Reference voltage (+)	AV_{REFP}			1.6		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD0}	V
	V_{BGR}	2.4 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

(Omitted)

Correct:

(2) When AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AV_{REF} (–) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI16 to ANI26

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Notes 1, 2	AINL	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±8.5	LSB
Conversion time	t_{CONV}	(Omitted)					
Zero-scale error Notes 1, 2	EZS						
Full-scale error Notes 1, 2	EFS						
Integral linearity error Note 1	ILE						
Differential linearity error Note 1	DLE						
Reference voltage (+)	AV_{REFP}			1.6		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD0}	V
	V_{BGR}	2.4 V ≤ V_{DD} ≤ 5.5 V	HS mode	1.38	1.45	1.5	V

(Omitted)

Condition of (3) When AVREF (+) = VDD, AVREF (–) = VSS, target ANI pin : ANI0 to ANI14, ANI16 to ANI26 added (page 1034)

Incorrect:

(3) When $AV_{REF\ (+)}$ = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF\ (-)}$ = V_{SS} (ADREFM = 0), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Notes 1, 2]	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±10.5	LSB
Conversion time	t_{CONV}	(Omitted)					
Zero-scale error[Notes 1, 2]	EZS						
Full-scale error[Notes 1, 2]	EFS						
Integral linearity error[Note 1]	ILE						
Differential linearity error[Note 1]	DLE						
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI26		0		EV_{DD0}	V
	V_{BGR}	**2.4 V ≤ V_{DD} ≤ 5.5 V**		1.38	1.45	1.5	V

(Omitted)

Correct:

(3) When $AV_{REF\,(+)}$ = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF\,(-)}$ = V_{SS} (ADREFM = 0), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Notes 1, 2]	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±10.5	LSB
Conversion time	t_{CONV}	(Omitted)					
Zero-scale error[Notes 1, 2]	EZS						
Full-scale error[Notes 1, 2]	EFS						
Integral linearity error[Note 1]	ILE						
Differential linearity error[Note 1]	DLE						
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI26		0		EV_{DD0}	V
	V_{BGR}	2.4 V ≤ V_{DD} ≤ 5.5 V	HS mode	1.38	1.45	1.5	V

(Omitted)

Condition of (4) When AVREF (+) = Internal reference voltage, AVREF (–) = AVREFM/ANI1, target ANI pin : ANI0 to ANI14, ANI16 to ANI26 added (page 1035)

Incorrect:

(4) When $AV_{REF\ (+)}$ = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), $AV_{REF\ (-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

(T_A = –40 to +85°C, **$1.6\ V \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\ V$**, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V, Reference voltage (+) = V_{BGR}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		bit
Conversion time	t_{CONV}	8-bit resolution	$2.4\ V \leq V_{DD} \leq 5.5\ V$	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution	$2.4\ V \leq V_{DD} \leq 5.5\ V$			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	$2.4\ V \leq V_{DD} \leq 5.5\ V$			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution	$2.4\ V \leq V_{DD} \leq 5.5\ V$			±1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.5	V
Reference voltage (–)	AV_{REFM}				V_{SS}		V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

(Omitted)

Correct:

(4) When $AV_{REF\ (+)}$ = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), $AV_{REF\ (-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

(T_A = –40 to +85°C, $2.4\ V \leq V_{DD} \leq 5.5\ V$, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V, Reference voltage (+) = V_{BGR}, Reference voltage (–) = AV_{REFM} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		bit
Conversion time	t_{CONV}	8-bit resolution	$2.4\ V \leq V_{DD} \leq 5.5\ V$	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution	$2.4\ V \leq V_{DD} \leq 5.5\ V$			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	$2.4\ V \leq V_{DD} \leq 5.5\ V$			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution	$2.4\ V \leq V_{DD} \leq 5.5\ V$			±1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.5	V
Reference voltage (–)	AV_{REFM}				V_{SS}		V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

(Omitted)

14. Condition of Temperature sensor characteristics in Electrical Specifications chapter (section 29.7.2) added (page 1036)

Incorrect:

29.7.2 Temperature sensor characteristics

(T_A = –40 to +85°C, **2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V**, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/C
Operation stabilization wait time	t_{AMP}				5	μs

Correct:

29.7.2 Temperature sensor characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/C
Operation stabilization wait time	t_{AMP}				5	μs

15. Industrial applications and extended-temperature products released

Industrial applications and extended-temperature products released (p.5)

Added:

Figure 1-1. Part Number, Memory Size, and Package of RL78/G13

Part No. R 5 F 1 0 0 L E A x x x F B

Package type:
- SP : SSOP, 0.65 mm pitch
- FP : LQFP, 0.80 mm pitch
- FA : LQFP, 0.65 mm pitch
- FB : LQFP, 0.50 mm pitch
- NA : WQFN, 0.50 mm pitch
- LA : LGA, 0.50 mm pitch
- BG : FBGA, 0.40 mm pitch

ROM number (Omitted with blank products)

Classification:
- A : Consumer applications, operating ambient temperature : -40˚C to 85˚C
- D : Industrial applications, operating ambient temperature : -40˚C to 85˚C

ROM capacity:
- A : 16 KB
- C : 32 KB
- D : 48 KB
- E : 64 KB
- F : 96 KB
- G : 128 KB
- H : 192 KB
- J : 256 KB
- K : 384 KB
- L : 512 KB

Pin count:
- A : 20 to 30-pin
- B : 32-pin
- C : 36-pin
- E : 40-pin
- F : 44-pin
- G : 48-pin
- J : 52-pin
- L : 64-pin
- M : 80-pin
- P : 100-pin
- S : 128-pin

RL78/G13 group
- 100 : Data flash is provided
- 101 : Data flash is not provided

Memory type:
- F : Flash memory

Renesas MCU

Renesas semiconductor product

Remark For details about extended-temperature products (operating ambient temperature: –40°C to 105°C), contact a Renesas Electronics Corporation or an authorized Renesas Electronics Corporation distributor.

IOH spec of products for industrial application in DC characteristics of ELECTRICAL SPECIFICATIONS added (p.988)

Incorrect:

29.4.1 Pin characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV_{DD0} ≤ 5.5 V			–10.0 Note 2	mA
		(Omitted)					
		Total of all pins (When duty = 70% Note 3)	1.6 V ≤ EV_{DD0} ≤ 5.5 V			–135.0	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V_{DD} ≤ 5.5 V			–0.1 Note 2	mA
		Total of all pins (When duty = 70% Note 3)	1.6 V ≤ V_{DD} ≤ 5.5 V			–1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

(Omitted)

Correct:

29.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV_{DD0} ≤ 5.5 V			–10.0 Note 2	mA
		(Omitted)					
		Total of all pins (When duty = 70% Note 3)	1.6 V ≤ EV_{DD0} ≤ 5.5 V			–135.0 Note 4	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V_{DD} ≤ 5.5 V			–0.1 Note 2	mA
		Total of all pins (When duty = 70% Note 3)	1.6 V ≤ V_{DD} ≤ 5.5 V			–1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

(Omitted)

4. The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx) is –100 mA.

16. Incorrect descriptions of recommended connection of unused pins of P60 to P63 in table 2-3 in pin functions chapter revised (p.93)

Incorrect:

Table 2-3. Connection of Unused Pins (128-pin products) (2/4)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
(Omitted)			
P60/SCLA0	13-R	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. **Output: Leave open.**
P61/SDAA0			
P62/SCLA1			
P63/SDAA1			
P64/TI10/TO10	8-R		
P65/TI11/TO11			
P66/TI12/TO12			
P67/TI13/TO13			

Correct:

Table 2-3. Connection of Unused Pins (128-pin products) (2/4)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
(Omitted)			
P60/SCLA0	13-R	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Set the port's output latch to 0 and leave the pins open, or set the port's output latch to 1 and independently connect the pins to EV_{DD0} and EV_{DD1} or EV_{SS0} and EV_{SS1} via a resistor.
P61/SDAA0			
P62/SCLA1			
P63/SDAA1			
P64/TI10/TO10	8-R		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P65/TI11/TO11			
P66/TI12/TO12			
P67/TI13/TO13			

17. Incorrect descriptions of 7.4.2 Shifting to HALT/STOP mode after starting operation in real-time clock chapter revised (p.449)

Incorrect:

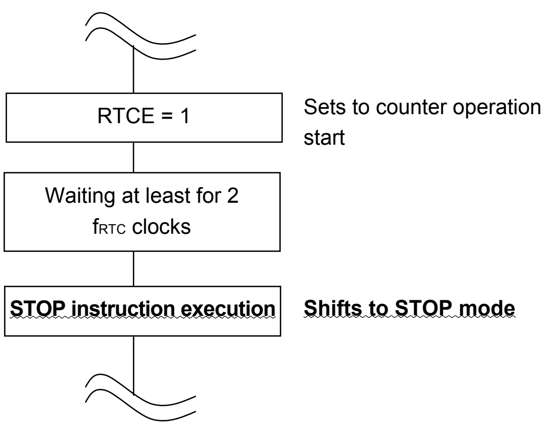
7.4.2 Shifting to **STOP mode** after starting operation

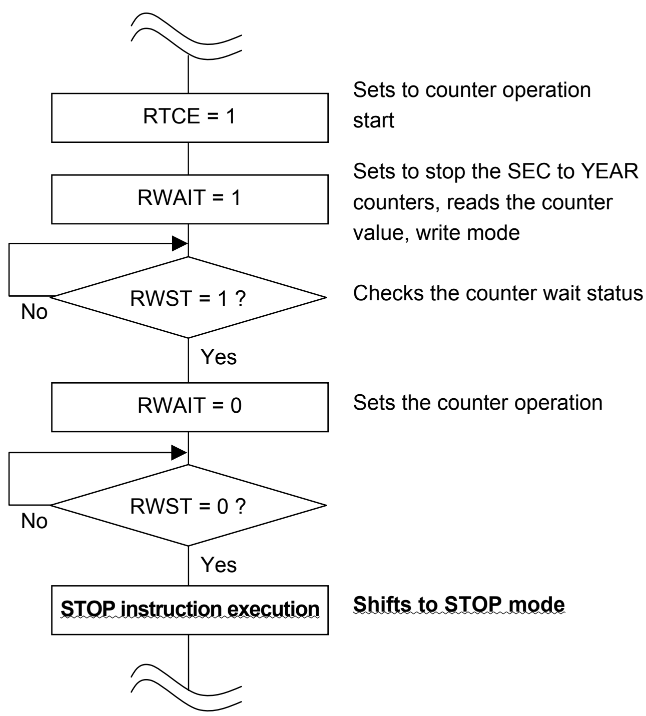
Perform one of the following processing when shifting to **STOP mode** immediately after setting the RTCE bit to 1.

However, after setting the RTCE bit to 1, this processing is not required when shifting to **STOP mode** after the INTRTC interrupt has occurred.

- Shifting to **STOP mode** when at least two input clocks (f_{RTC}) have elapsed after setting the RTCE bit to 1 (see Figure 7-18, Example 1).
- Checking by polling the RWST bit to become 1, after setting the RTCE bit to 1 and then setting the RWAIT bit to 1. Afterward, setting the RWAIT bit to 0 and shifting to **STOP mode** after checking again by polling that the RWST bit has become 0 (see Figure 7-18, Example 2).

Figure 7-18. Procedure for Shifting to **STOP Mode** After Setting RTCE bit to 1





Correct:

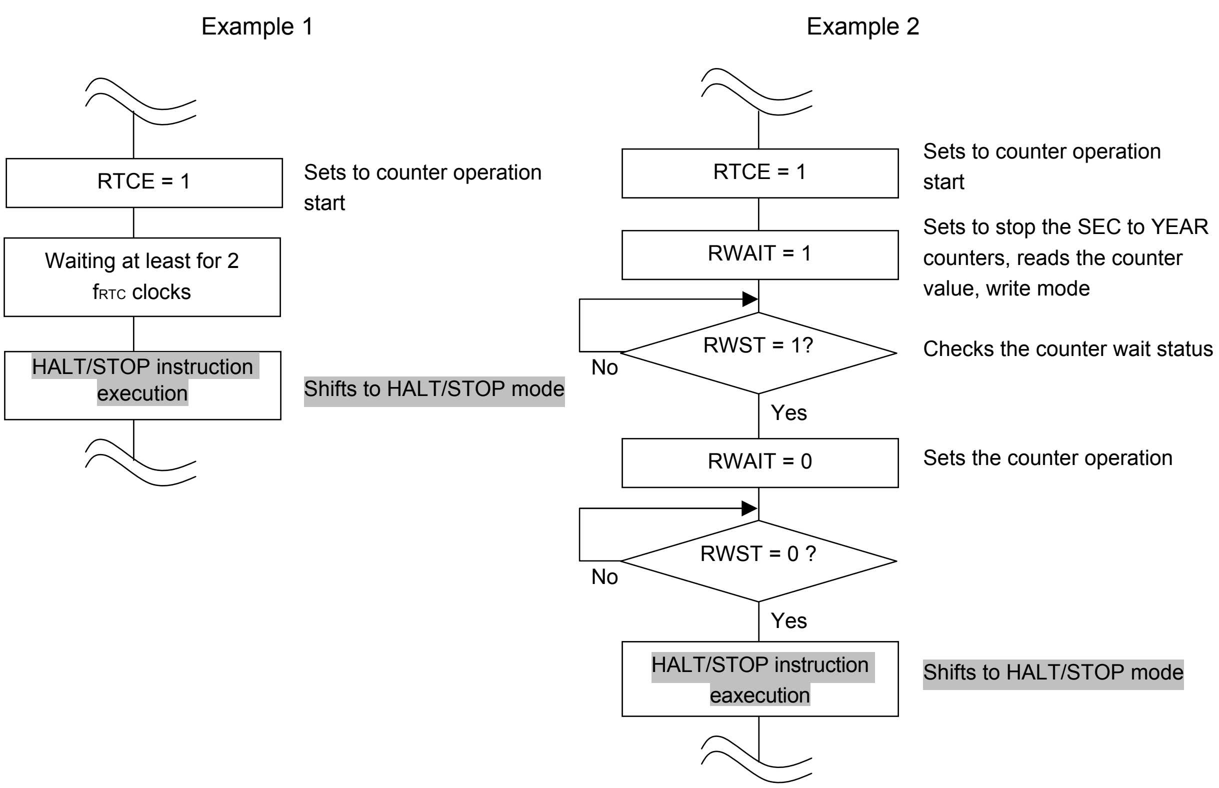
7.4.2 Shifting to HALT/STOP mode after starting operation

Perform one of the following processing when shifting to HALT/STOP mode immediately after setting the RTCE bit to 1.

However, after setting the RTCE bit to 1, this processing is not required when shifting to HALT/STOP mode after the INTRTC interrupt has occurred.

- Shifting to HALT/STOP mode when at least two input clocks (f_{RTC}) have elapsed after setting the RTCE bit to 1 (see Figure 7-18, Example 1).
- Checking by polling the RWST bit to become 1, after setting the RTCE bit to 1 and then setting the RWAIT bit to 1. Afterward, setting the RWAIT bit to 0 and shifting to HALT/STOP mode after checking again by polling that the RWST bit has become 0 (see Figure 7-18, Example 2).

Figure 7-18. Procedure for Shifting to HALT/STOP Mode After Setting RTCE bit to 1



18. Incorrect descriptions of reset processing time/standby mode release time revised

Incorrect descriptions of reset processing time revised (p.308, 861, 866, 871, 872, 883, 884)

Incorrect:

Reset processing time of reset by POR when the power is turned on

Reset processing time: 387 to 720 μs (When LVD is used)
155 to 407 μs (When LVD off)

Reset processing time when HALT reset or STOP reset

Reset processing time: 387 to 720 μs (When LVD is used)
155 to 407 μs (When LVD off)

Reset processing time when RESET input

Reset processing time: 387 to 674 μs (When LVD is used)
155 to 360 μs (When LVD off)

Correct:

Reset processing time of reset by POR when the power is turned on

Reset processing time: 497 to 720 μs (When LVD is used)
265 to 407 μs (When LVD off)

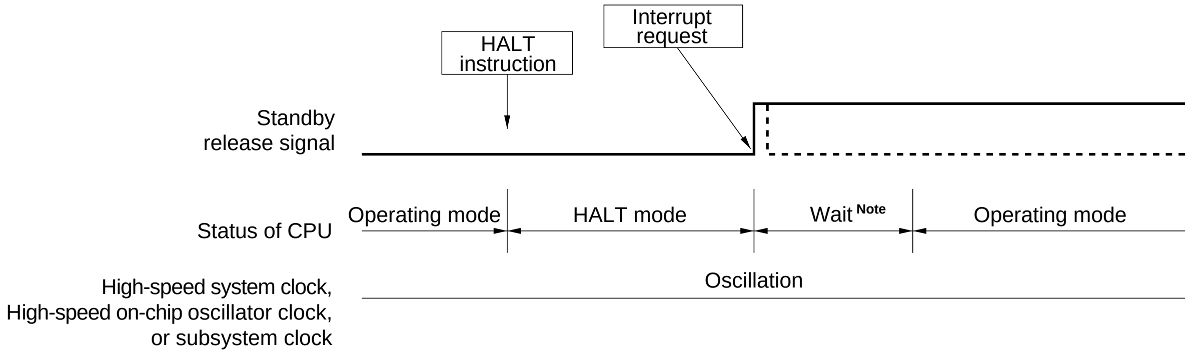
Reset processing time when HALT reset or STOP reset or RESET input

Reset processing time: 388 to 673 μs (When LVD is used)
156 to 360 μs (When LVD off)

Incorrect descriptions of HALT mode release time revised (p.860)

Incorrect:

Figure 18-3. HALT Mode Release by Interrupt Request Generation

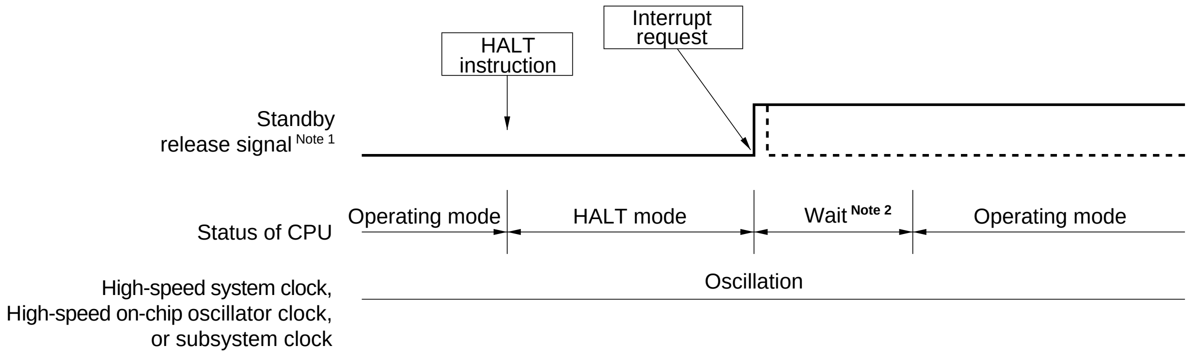


Note Wait time for HALT mode release

- **When vectored interrupt servicing is carried out**
  - **Main system clock: 13 to 15 clock**
  - **Subsystem clock (RTCLPC = 0): 8 to 10 clock**
  - **Subsystem clock (RTCLPC = 1): 9 to 11 clock**
- **When vectored interrupt servicing is not carried out**
  - **Main system clock: 8 to 9 clock**
  - **Subsystem clock (RTCLPC = 0): 3 to 4 clock**
  - **Subsystem clock (RTCLPC = 1): 4 to 5 clock**

Correct:

Figure 18-3. HALT Mode Release by Interrupt Request Generation



Notes 1. For details of the standby release signal, see Figure 16-1

2. Wait time for HALT mode release

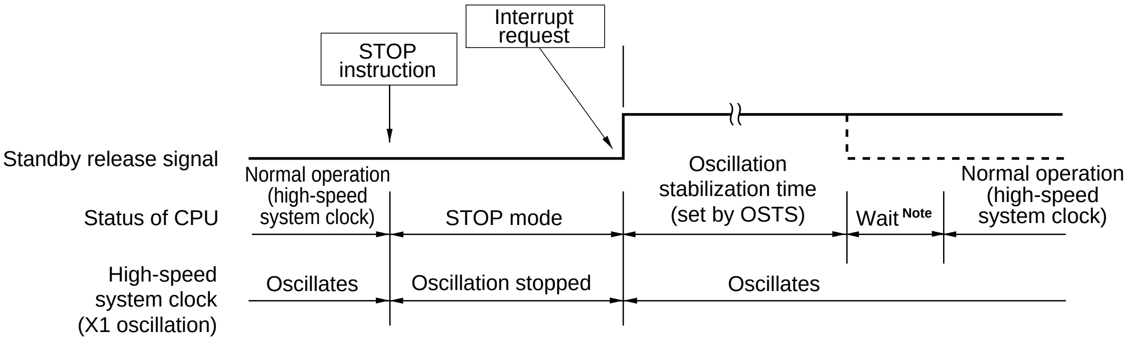
- When vectored interrupt servicing is carried out
  - Main system clock: 15 to 16 clock
  - Subsystem clock (RTCLPC = 0): 10 to 11 clock
  - Subsystem clock (RTCLPC = 1): 11 to 12 clock
- When vectored interrupt servicing is not carried out
  - Main system clock: 9 to 10 clock
  - Subsystem clock (RTCLPC = 0): 4 to 5 clock
  - Subsystem clock (RTCLPC = 1): 5 to 6 clock

Incorrect descriptions of STOP mode release time revised (p.864, 865)

Incorrect:

Figure 18-5. STOP Mode Release by Interrupt Request Generation (1/2)

(1) When high-speed system clock (X1 oscillation) is used as CPU clock

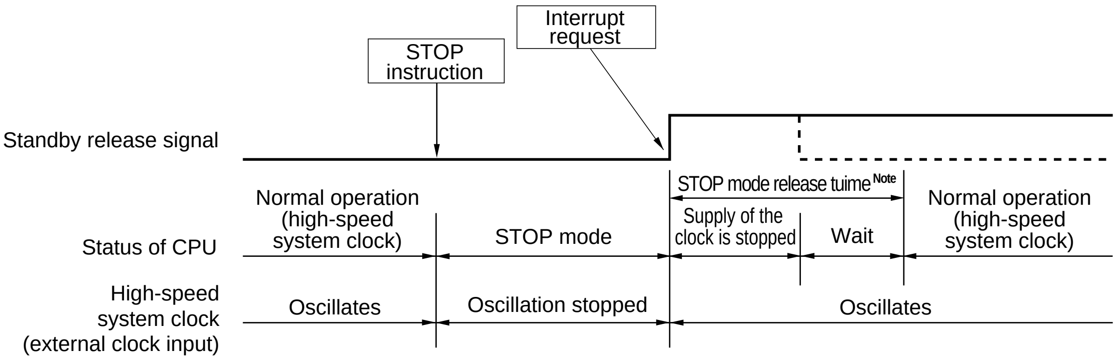


Note Wait time for STOP mode release

- **High-speed system clock (X1 oscillation): 3-clock**

Figure 18-5. STOP Mode Release by Interrupt Request Generation (2/2)

(2) When high-speed system clock (external clock input) is used as CPU clock



(3) When high-speed on-chip oscillator clock is used as CPU clock

(Omitted)

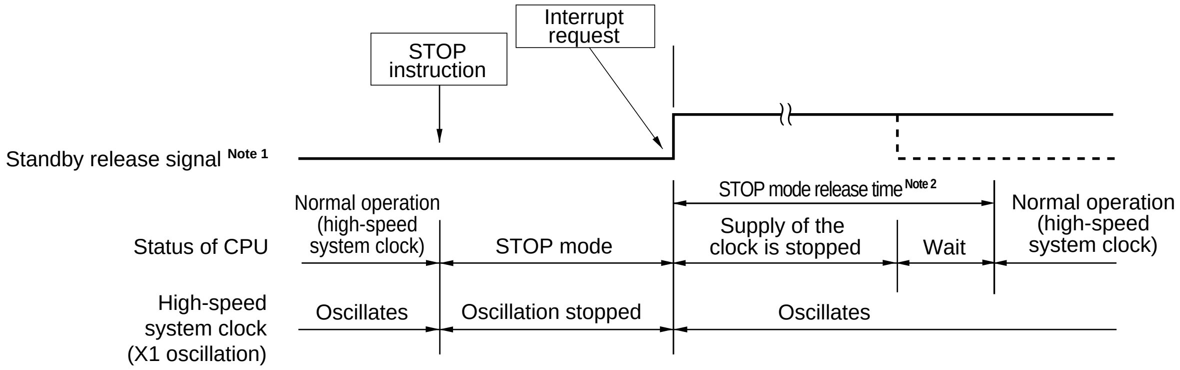
Note STOP mode release time:

- **High-speed system clock (external clock input): 19.1 to 31.98 μs**
- **High-speed on-chip oscillator clock: 19.1 to 31.98 μs**

Correct:

Figure 18-5. STOP Mode Release by Interrupt Request Generation (1/2)

(1) When high-speed system clock (X1 oscillation) is used as CPU clock



Notes 1. For details of the standby release signal, see Figure 16-1

2. STOP mode release time

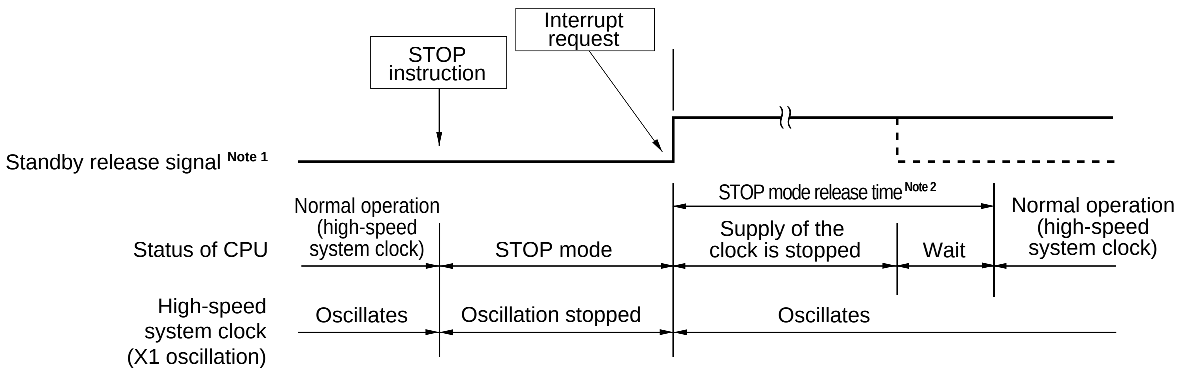
Supply of the clock is stopped: 18.96 μs to "whichever is longer 28.95 μs and the oscillation stabilization time (set by OSTS)"

Wait

- When vectored interrupt servicing is carried out: 10 to 11 clocks
- When vectored interrupt servicing is not carried out: 4 to 5 clocks

Figure 18-5. STOP Mode Release by Interrupt Request Generation (2/2)

(2) When high-speed system clock (external clock input) is used as CPU clock



(3) When high-speed on-chip oscillator clock is used as CPU clock

(Omitted)

Notes 1. For details of the standby release signal, see Figure 16-1

2. STOP mode release time

Supply of the clock is stopped: 19.08 to 32.99 μs

Wait

- When vectored interrupt servicing is carried out: 7 clocks
- When vectored interrupt servicing is not carried out: 1 clock

Explanations of SNOOZE mode shift time added (p.867)

Incorrect:

18.2.3 SNOOZE mode

(1) SNOOZE mode setting and operating statuses

(Omitted)

Correct:

18.2.3 SNOOZE mode

(1) SNOOZE mode setting and operating statuses

(Omitted)

In SNOOZE mode transition, wait status to be only following time.

From STOP to SNOOZE

HS (High-speed main) mode : 18.96 to 28.95 μs

LS (Low-speed main) mode : 20.24 to 28.95 μs

LV (Low-voltage main) mode : 20.98 to 28.95 μs

From SNOOZE to normal operation

- When vectored interrupt servicing is carried out:
  - HS (High-speed main) mode : 6.79 to 12.4 μs + 7 clocks
  - LS (Low-speed main) mode : 2.58 to 7.8 μs + 7 clocks
  - LV (Low-voltage main) mode : 12.45 to 17.3 μs + 7 clocks
- When vectored interrupt servicing is not carried out:
  - HS (High-speed main) mode : 6.79 to 12.4 μs + 1 clock
  - LS (Low-speed main) mode : 2.58 to 7.8 μs + 1 clock
  - LV (Low-voltage main) mode : 12.45 to 17.3 μs + 1 clock

19. Explanations of when using SNOOZE mode in A/D converter chapter added

Explanations of A/D converter mode register 2 (ADM2) added (p.493, 494)

Incorrect:

(4) A/D converter mode register 2 (ADM2)

(Omitted)

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage (1.45 V)
1	1	Setting prohibited

- When ADREFP1 or ADREFP0 bit is rewritten, this must be configured in accordance with the following procedures.
  (1) Set ADCE = 0
  (2) Change the values of ADREFP1 and ADREFP0
  (3) Stabilization wait time (A)
  (4) Set ADCE = 1
  (5) Stabilization wait time (B)
  When ADREFP1 and ADREFP0 are set to 1 and 0, the setting is changed to A = 1 μs, B = 5 μs.
  When ADREFP1 and ADREFP0 are set to 0 and 0 or 0 and 1, A needs no wait and B = 1 μ s.
- When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output.
  Be sure to perform A/D conversion while ADISS = 0.

AWC	Specification of the SNOOZE mode
0	Do not use the SNOOZE mode function.
1	Use the SNOOZE mode function.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

- The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f_{CLK}). If any other clock is selected, specifying this mode is prohibited.
- Using the SNOOZE mode function in the software trigger mode or hardware trigger no-wait mode is prohibited.
- Using the SNOOZE mode function in the sequential conversion mode is prohibited.
- **When using the SNOOZE mode function, specify a hardware trigger interval of at least "A/D conversion time with stabilization wait time" listed for Table 11-3.**

Correct:

(4) A/D converter mode register 2 (ADM2)

(Omitted)

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage (1.45 V) Note
1	1	Setting prohibited

- When ADREFP1 or ADREFP0 bit is rewritten, this must be configured in accordance with the following procedures.
  (1) Set ADCE = 0
  (2) Change the values of ADREFP1 and ADREFP0
  (3) Stabilization wait time (A)
  (4) Set ADCE = 1
  (5) Stabilization wait time (B)
  When ADREFP1 and ADREFP0 are set to 1 and 0, the setting is changed to A = 5 μs, B = 1 μs.
  When ADREFP1 and ADREFP0 are set to 0 and 0 or 0 and 1, A needs no wait and B = 1 μ s.
  After (5) stabilization time, start the A/D conversion.
- When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output and internal reference voltage output.
  Be sure to perform A/D conversion while ADISS = 0.

AWC	Specification of the SNOOZE mode
0	Do not use the SNOOZE mode function.
1	Use the SNOOZE mode function.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

- The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f_{CLK}). If any other clock is selected, specifying this mode is prohibited.
- Using the SNOOZE mode function in the software trigger mode or hardware trigger no-wait mode is prohibited.
- Using the SNOOZE mode function in the sequential conversion mode is prohibited.
- When using the SNOOZE mode function, specify a hardware trigger interval of at least "shift time to SNOOZE mode Note + A/D power supply stabilization wait time + A/D conversion time +2 f_{CLK} clock"
- Even when using SNOOZE mode, be sure to set the AWC bit to 0 in normal operation mode and change it to 1 just before shifting to STOP mode.
  Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation mode.
  If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE or normal operation mode.

Note Refer to "From STOP to SNOOZE" in 18.2.3 SNOOZE mode

Explanations of SNOOZE mode related to A/D converter added (p.526)

Incorrect:

(1) If an interrupt is generated after A/D conversion ends

(Omitted)

- While in the select mode

After A/D conversion ends and the A/D conversion end interrupt request signal (INTAD) is generated, the clock request signal remains at the high level, and the A/D converter switches from the SNOOZE mode to the normal operation mode. To stop the high-speed on-chip oscillator clock supplied while in the SNOOZE mode, clear bit 2 (AWC) of A/D converter mode register 2 (ADM2) to 0. Doing this sets the clock request signal (an internal signal) to the low level and stops the supply of the high-speed on-chip oscillator clock.

- While in the scan mode

If even one A/D conversion end interrupt request signal (INTAD) is generated during A/D conversion of the four channels, the clock request signal remains at the high level, and the A/D converter switches from the SNOOZE mode to the normal operation mode. To stop the high-speed on-chip oscillator clock supplied while in the SNOOZE mode, clear bit 2 (AWC) of A/D converter mode register 2 (ADM2) to 0. Doing this sets the clock request signal (an internal signal) to the low level and stops the supply of the high-speed on-chip oscillator clock.

Correct:

(1) If an interrupt is generated after A/D conversion ends

(Omitted)

- While in the select mode

When A/D conversion ends and an A/D conversion end interrupt request signal (INTAD) is generated, the A/D converter returns to normal operation mode from SNOOZE mode. At this time, be sure to clear bit 2 (AWC = 0: SNOOZE mode release) of the A/D converter mode register 2 (ADM2). If the AWC bit is left set to 1, A/D conversion will not start normally in the subsequent SNOOZE or normal operation mode.

- While in the scan mode

If even one A/D conversion end interrupt request signal (INTAD) is generated during A/D conversion of the four channels, the clock request signal remains at the high level, and the A/D converter switches from the SNOOZE mode to the normal operation mode. At this time, be sure to clear bit 2 (AWC = 0: SNOOZE mode release) of A/D converter mode register 2 (ADM2) to 0. If the AWC bit is left set to 1, A/D conversion will not start normally in the subsequent SNOOZE or normal operation mode.

20. Caution of when using SNOOZE mode in serial array unit added

Explanations of SNOOZE mode related to CSI added (p.631, 633)

Incorrect:

(Omitted)

Caution Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, be sure to set the STm0 bit to 1 and clear the SEm0 bit (to stop the operation).

Correct:

(Omitted)

Caution Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm0 bit to 1 (clear the SEm0 bit, and stop the operation).
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).

Explanations of SNOOZE mode related to UART added (p.658, 659, 661)

Incorrect:

(Omitted)

Caution Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, be sure to set the STm1 bit to 1 and clear the SEm1 bit (to stop the operation).

Correct:

(Omitted)

Caution Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm1 bit to 1 (clear the SEm1 bit, and stop the operation).
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).

21. Explanations of data flash in flash memory chapter added (p.938)

Incorrect:

An overview of the data flash memory is provided below.

- The data flash memory can be written to by using the flash memory programmer or an external device
- Programming is performed in 8-bit units
- Blocks can be deleted in 1 KB units
- The only access by CPU instructions is byte reading **(reading: four clock cycles)**

(Omitted)

Correct:

An overview of the data flash memory is provided below.

- The data flash memory can be written to by using the flash memory programmer or an external device
- Programming is performed in 8-bit units
- Blocks can be deleted in 1 KB units
- The only access by CPU instructions is byte reading (1 clock cycle + wait 3 clock cycles)

(Omitted)

- When data flash is accessed, the CPU waits for three clock cycles

22. Spec of On-chip oscillator characteristics in electrical specifications chapter confirmed (p.983)

Incorrect:

29.3.2 On-chip oscillator characteristics

(T_A = –20 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note	f_{IH}	1.8 V ≤ V_{DD} ≤ 5.5 V	32 MHz selected	31.68	32.00	32.32	MHz
			24 MHz selected	23.76	24.00	24.24	MHz
			(Omitted)				
		1.6 V ≤ V_{DD} < 1.8 V	32 MHz selected	30.40	32.00	33.60	MHz
			24 MHz selected	22.80	24.00	25.20	MHz
			(Omitted)				

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note	f_{IH}	1.8 V ≤ V_{DD} ≤ 5.5 V	32 MHz selected	31.52	32.00	32.48	MHz
			24 MHz selected	23.64	24.00	24.36	MHz
			(Omitted)				
		1.6 V ≤ V_{DD} < 1.8 V	32 MHz selected	30.24	32.00	33.76	MHz
			24 MHz selected	22.68	24.00	25.32	MHz
			(Omitted)				

Note This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

When WQFN (24-, 32-, 40-, 48-pin), FLGA (25-, 36-pin), FBGA (64-pin), TQFP (64-pin), LQFP (14 × 20) (100-, 128-pin) products, these specifications show target values, which may change after device evaluation.

29.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note 1	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy Note 2		–20 to +85 °C	1.8 V≤V_{DD}≤5.5 V	–1		+1	%
			1.6 V≤V_{DD}<1.8 V	–5		+5	%
		–40 to –20 °C	1.8 V≤V_{DD}≤5.5 V	–1.5		+1.5	%
			1.6 V≤V_{DD}<1.8 V	–5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

Issued Document History

RL78/G13 Incorrect description notice, issued document history

Document Number	Issue Date	Description
TN-RL*-A001A/E	Dec. 5, 2011	First edition issued Incorrect descriptions of No.1 to No.10 revised
TN-RL*-A001B/E	Dec. 21, 2011	Rev.2.00 issued Revisions of No. 11 to No. 14 incorrect descriptions added
TN-RL*-A001C/E	Mar. 27, 2012	Rev.3.00 issued Revisions of No. 15 to No. 22 incorrect descriptions added (This notification)